ECE 6095 Spring 2019
Advanced Digital Systems Design

Tues/Thurs 12:30pm-1:45pm UTEB 175

***Course Description**: Three Credits.* Microarchitecture and design of hardware acceleration for domain-specific applications. Topics include gate-level design, register-transfer-level (RTL) design, microarchitecture, instruction set architecture, compilers, programming languages, and algorithms. Focus on both efficient software for embedded applications and the design of efficient hardware systems for such applications.

Instructor: Professor Omer Khan
Office: ITEB 447 Email: khan@uconn.edu
Office Hours: *appointment via email*
Course Website: http://www.engr.uconn.edu/~omer.khan/courses/ece6095_s19/index.html

Course Overview:
Today, the field of computer systems is a stack of abstraction and implementation layers with applications at the top and semiconductor technology at the bottom. The intermediate layers include devices, circuits, gate-level design, register-transfer-level (RTL) design, microarchitecture, instruction set architecture, compilers, operating systems, programming languages, and algorithms. Computer engineering is usually focused in the middle of this stack spanning circuits to operating systems. Recent focus has shifted from general-purpose computing to application-specific systems. In this era, hardware acceleration of domain specific applications has emerged as an important area of computer engineering. This course focuses on how to microarchitect and design *domain-specific designs*. Accordingly, the course caters both to students interested in writing efficient software for embedded applications, and to those interested in designing efficient hardware systems for such applications.

The (tentative) schedule for the course is as follows: (lectures same as ECE 3401)

- Logic Design Techniques and Hardware Description Language
- VHDL: Design Modeling, Simulation, Synthesis, and Verification
- State Machine (SM) Charts
- Microprogramming
- High Level Synthesis (HLS)
- High Level Design Examples, e.g., Microcontroller, Machine Learning
- Timing Synchronous and Computer-aided Design
- Verification and Testing of Digital Designs
- Programmable Logic Devices, e.g., FPGAs

Textbook (supplemental to lectures): *Available through UConn Bookstore*
Digital Systems Design Using VHDL by Charles H. Roth, Jr. and Lizy Kurian John, 3rd Edition

Grading Policy:	Midterm Exam #1	25% (tentative: late Mar)
	Midterm Exam #2	25% (tentative: late Apr)
	Project	50%

Software Tools:
This course has a lab and project component using VHDL and Xilinx Vivado tool-chains. Assignments will include designing and simulating hardware design modules using VHDL and HLS.

ECS learning center in rooms ITEB 134 and 138 have machines with the required software. The TA's office hours reflect the lab and project help hours as well.

Rules:

- Turn off all electronics during classes, including laptops, tablets, phones etc.
- Late assignments will ***not*** be accepted. We will check assignments for academic dishonesty.
- Participation in lab and project assignments is ***required*** to get a passing grade for the course.
- I strongly encourage you to form a group of up to two students and work together on the project. The project must be a quantitative microarchitectural evaluation of an algorithm or application using the HDL tool-chain (VHDL or HLS implementation). The algorithm/application must be designed by the students and optimized to achieve high performance and/or energy efficiency goals. The project related deadlines are required and no late submissions will be accepted (unless prior instructor consent is granted):

    - First Week March: 1-page project proposal due including your application's pseudo-code
    - End March: Project plan due (quantify all intermediate and final deliverables)
    - End April: Final deliverables and report due
    - Early May: Meet the instructor to present and discuss the project outcomes