Course Description: Three Credits. Prerequisite: CSE 2300. Design and evaluation of control and data structures for digital systems. Hardware design languages are used to describe and design alternative register transfer level architectures and control units with a micro-programming emphasis. Consideration of computer architecture, memories, digital interfacing timing and synchronization, and microprocessor systems.

Instructor: Professor Omer Khan  
Office: ITEB 447  Email: khan@uconn.edu  
Office Hours: Tuesday and Thursday 11am-Noon (only confirmed appointments via email)  
Course Website: http://www.engr.uconn.edu/~omer.khan/courses/ece3401_s20/index.html

TA: Mohsin Shan  
Email: mohsin.shan@uconn.edu  
Office Hours: Monday, Wednesday, and Friday 4-6pm ITE 138

Textbook (supplemental to lectures): Available through UConn Bookstore  
Digital Systems Design Using VHDL by Charles H. Roth, Jr. and Lizy Kurian John, 3rd Edition

Software Tools:  
This course has a programming component using VHDL software tool-chain. Assignments will include designing and simulating hardware design modules using VHDL.

ECS learning center in rooms ITEB 138 and 134 have machines with the required software. The TA’s office hours are aimed for you to get help on the programming and homework assignments.

UG Grading Policy:  
Programming & Homework Assignments 30%  
Midterm Exam #1 20% (tentative: early Mar)  
Midterm Exam #2 20% (tentative: early Apr)  
Final Exam 30%

GRAD Grading Policy:  
Programming & Homework Assignments 20%  
Midterm Exam #1 20% (tentative: early Mar)  
Midterm Exam #2 20% (tentative: early Apr)  
Project 40%

Rules:  
Participation in programming assignments is required to get a passing grade for the course. Late assignments will not be accepted. We will check assignments for academic dishonesty. Turn off all electronics during classes, including laptops, tablets, phones etc.
**GRAD Project:** I strongly encourage you to form a group of up to two students and work together on the project. The project must be a quantitative evaluation of an algorithm implementation in hardware using the VHDL tool-chain. The algorithm must also be implemented in software (e.g., a C implementation) for comparison to the hardware design. The software and hardware implementations must be tested using a set of functional test cases. A successful project must demonstrate functional correctness, as well as superior performance and/or energy efficiency for the hardware design. The project related deadlines are required and no late submissions will be accepted (unless prior written instructor consent is granted):

- Late Feb: Project proposal due including your algorithm’s pseudo-code and envisioned test cases. A clear outline of project plan and deliverables must also be included.
- Late March: Mid project in-person review
- End April: Final project in-person review
- Final Exam Week: Final project report due

**Tentative Schedule:**

- Logic Design Techniques and Hardware Description Language
- VHDL: Design Modeling, Simulation, Synthesis, and Verification
- State Machine (SM) Charts
- Microprogramming
- High Level Design Example of a Microcontroller
- Memory Design
- High Level Synthesis (HLS)
- Programmable Logic Devices
- Timing Synchronous and Computer-aided Design
- Verification and Testing of Digital Designs