

PA0 Guide

ECE 3401 – Spring 2021

Course TA contact information:

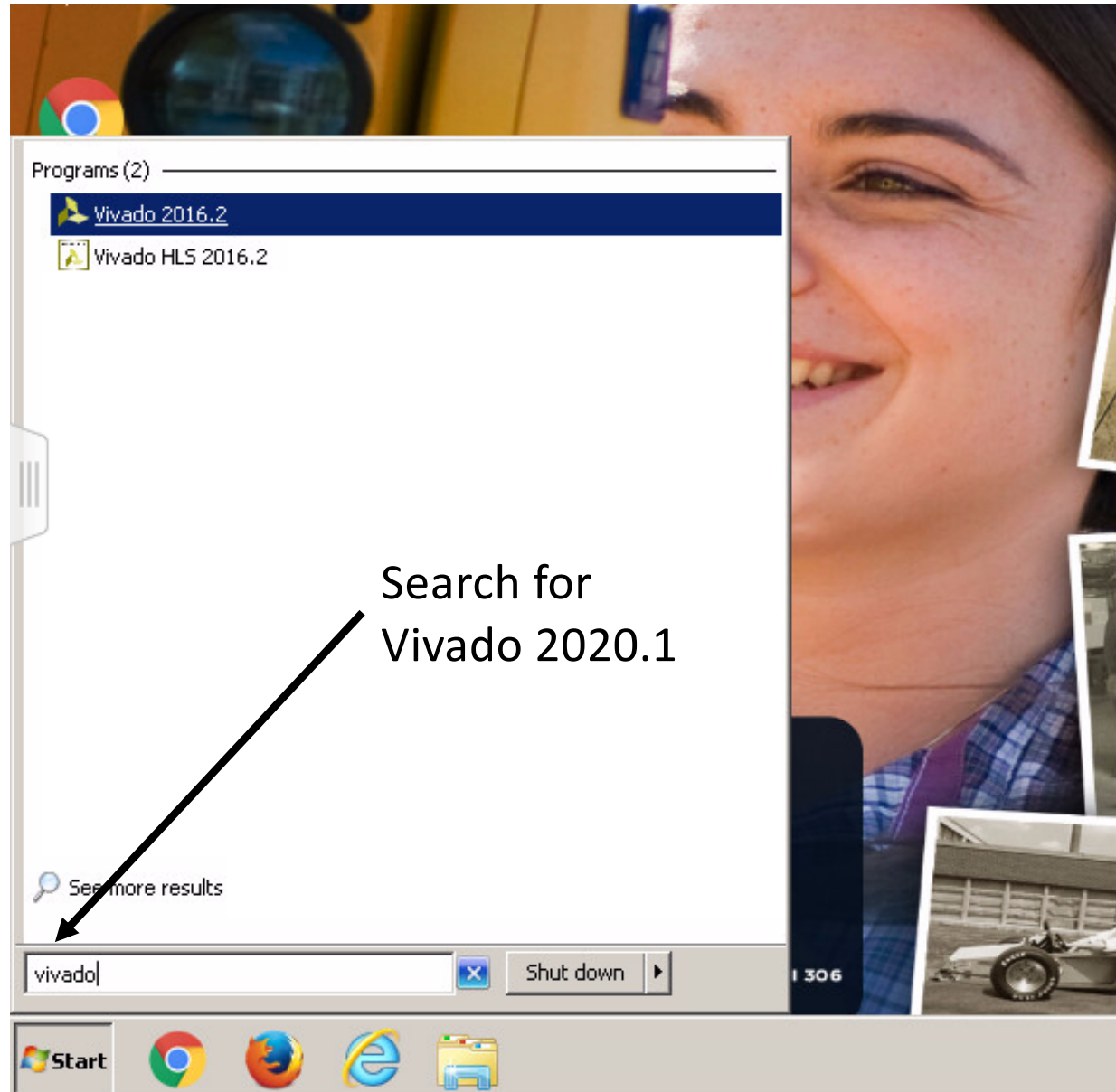
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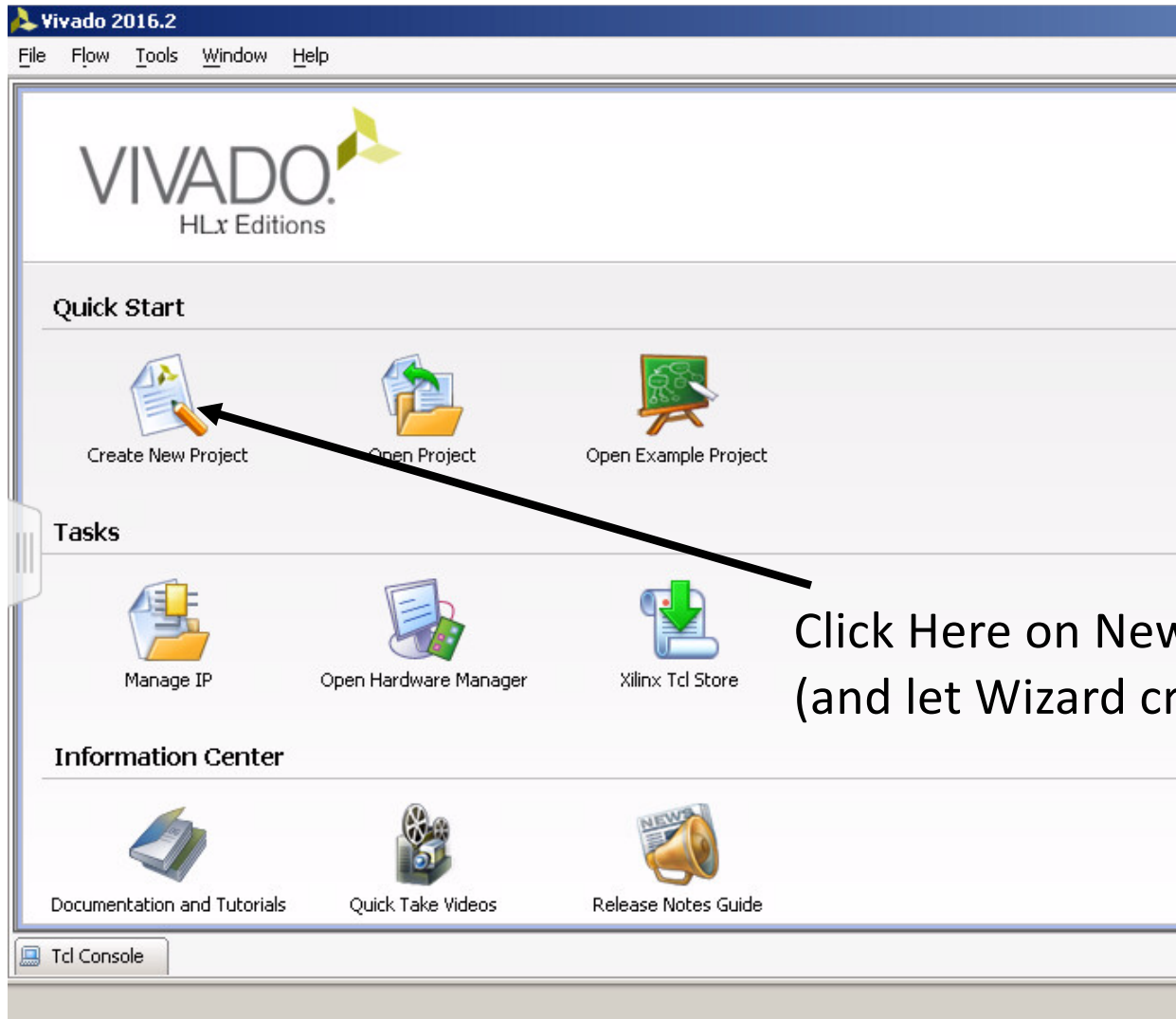
UConn AnyWare Login Steps

1. Open <https://software.uconn.edu/uconn-software-online/>
2. Click on the “Launch school specific desktops” icon under Launch AnyWare
3. Under the VMware Horizon: Enter your NetID as Username, and enter your password
4. When you login, you will be using “Engineering Desktop”. Click on the “Engineering Desktop”, and wait for you to get logged into the VM
5. On the left Window menu, select “Xilinx” at the end of the menu
6. Within Xilinx, click on “Vivado 2020.1” and wait for the tool to open

Start Vivado



Create a New Project



Project Wizard

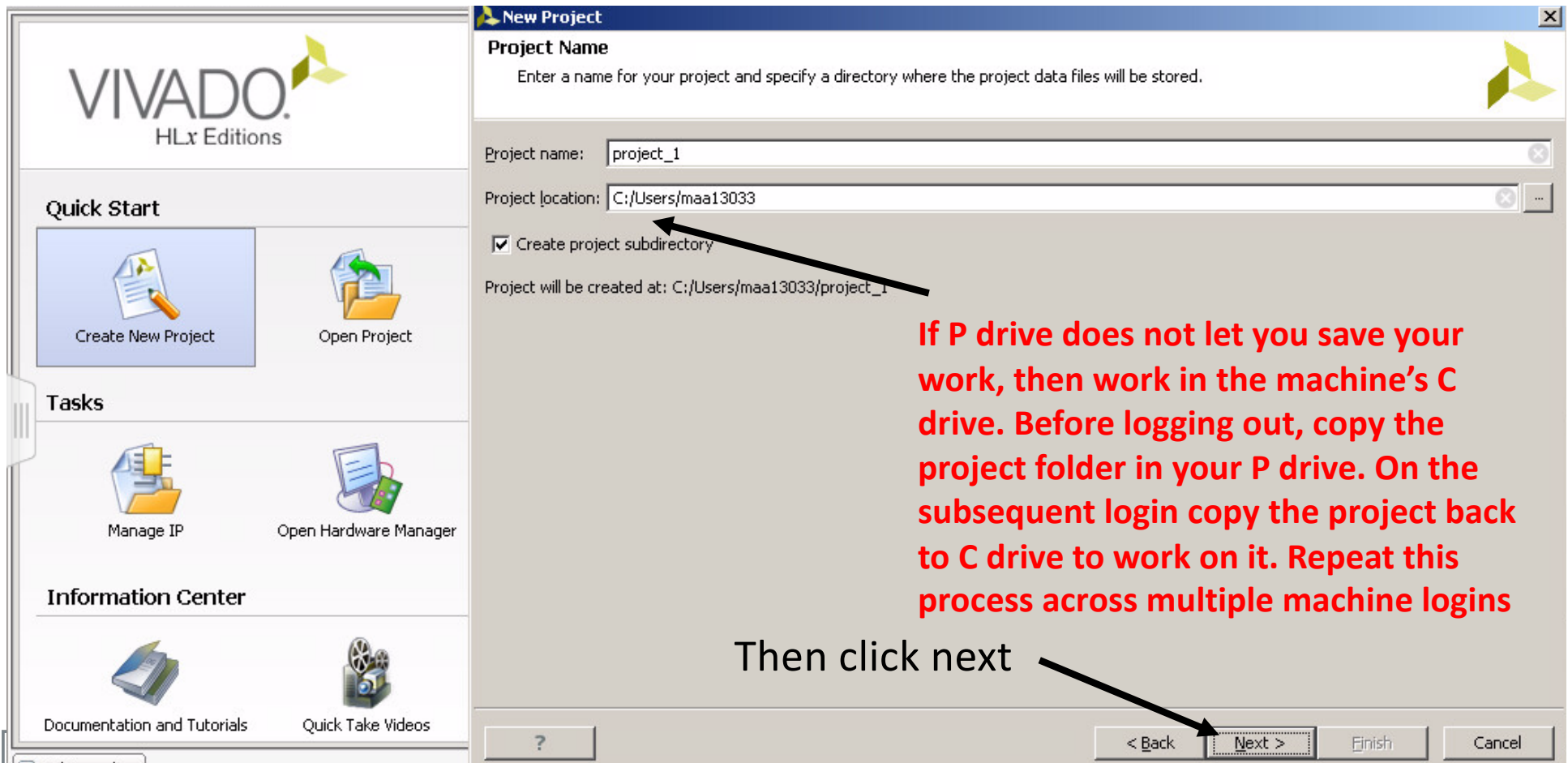
- The project wizard will open. Give any name to your project (e.g. lab0) and leave the rest as is

You can work from your P drive where data is saved across multiple machine logins

Then click next

Project Wizard

- The project wizard will open. Give any name to your project (e.g. lab0) and leave the rest as is



VIVADO
HLx Editions

Quick Start

Create New Project Open Project

Tasks

Manage IP Open Hardware Manager

Information Center

Documentation and Tutorials Quick Take Videos

New Project

Project Name
Enter a name for your project and specify a directory where the project data files will be stored.

Project name: project_1

Project location: C:/Users/maa13033

Create project subdirectory

Project will be created at: C:/Users/maa13033/project_1

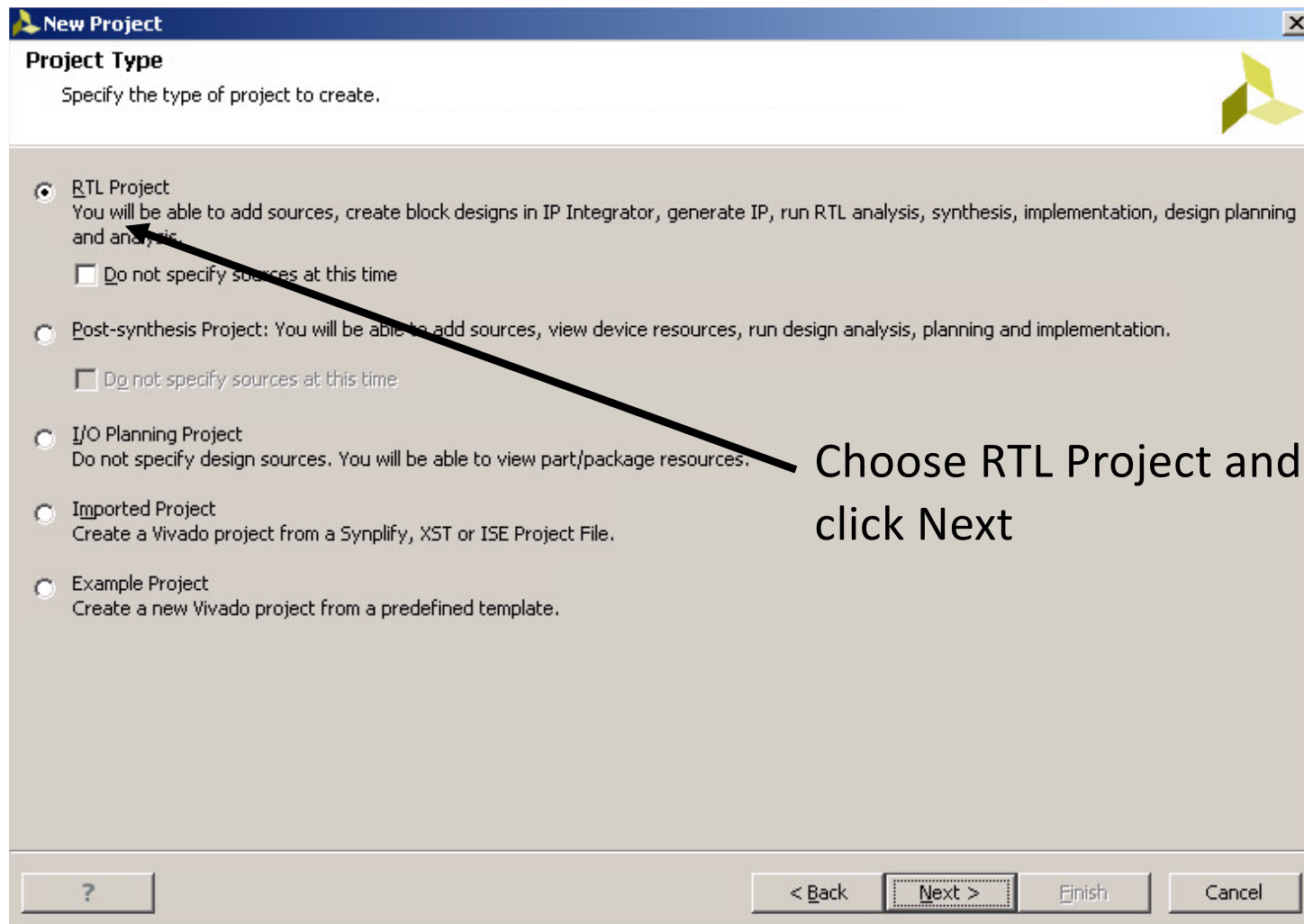
Then click next

< Back **Next >** Finish Cancel

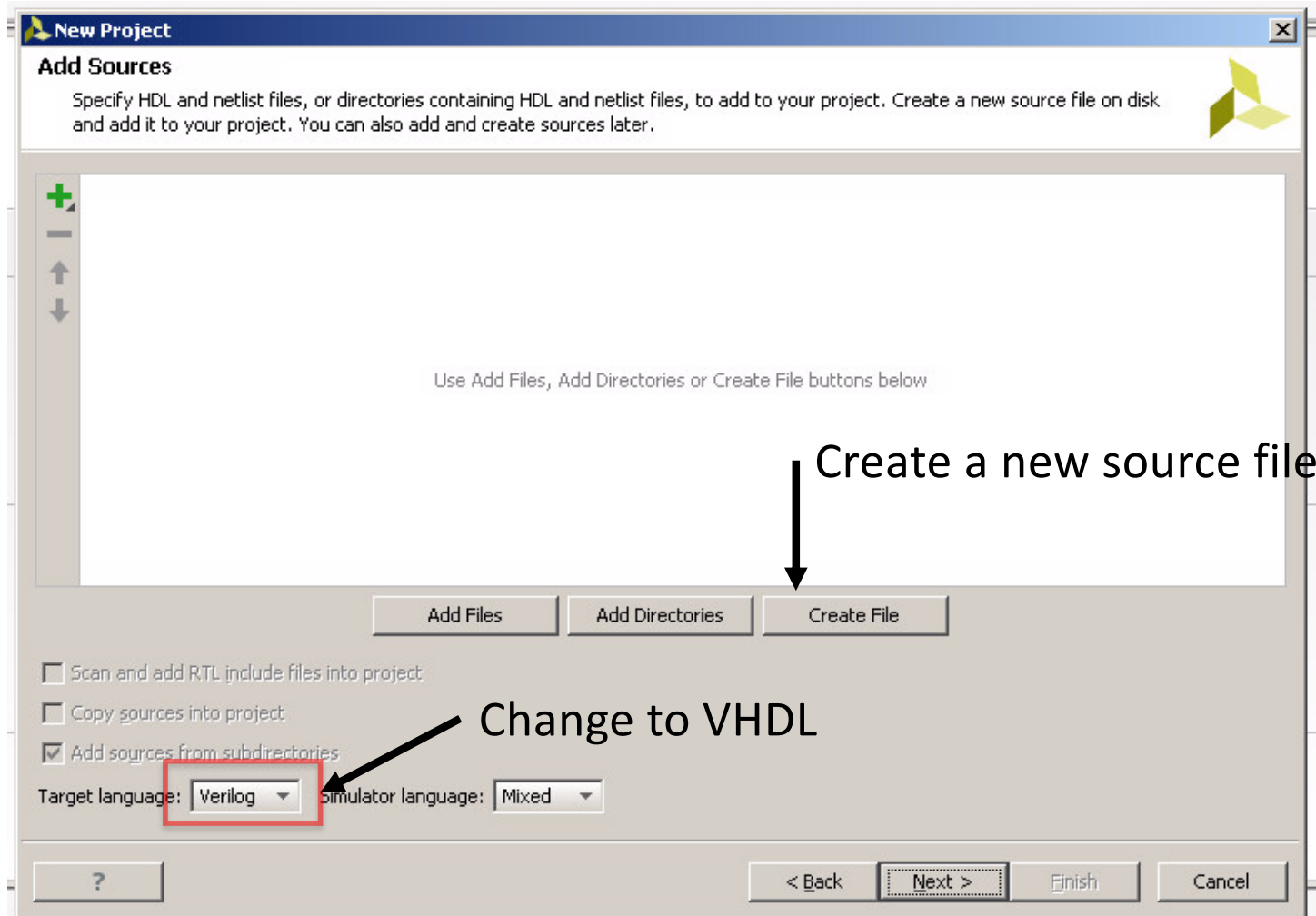
If P drive does not let you save your work, then work in the machine's C drive. Before logging out, copy the project folder in your P drive. On the subsequent login copy the project back to C drive to work on it. Repeat this process across multiple machine logins

Project Settings

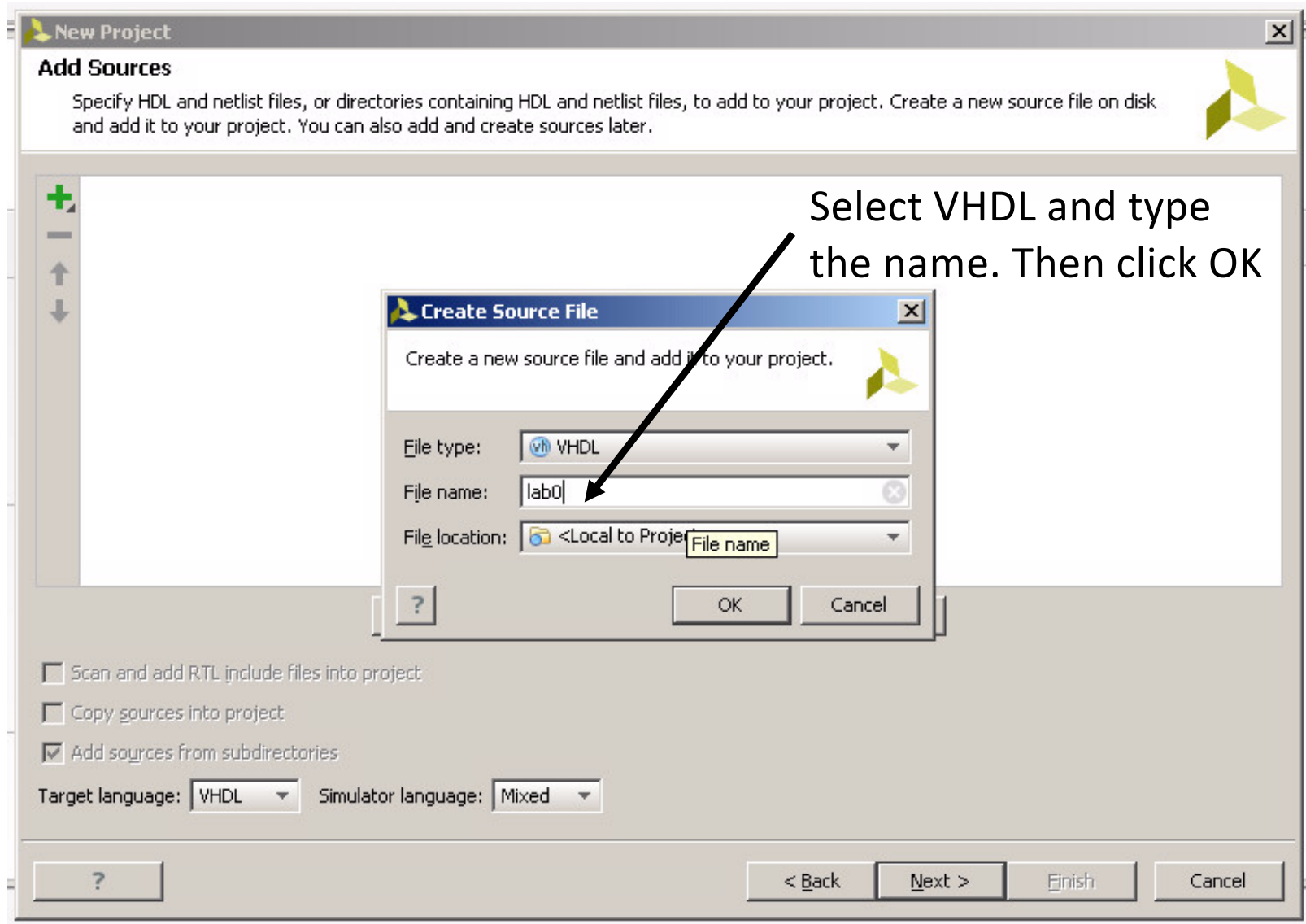
- Select RTL Project, then click next
- And then Finish



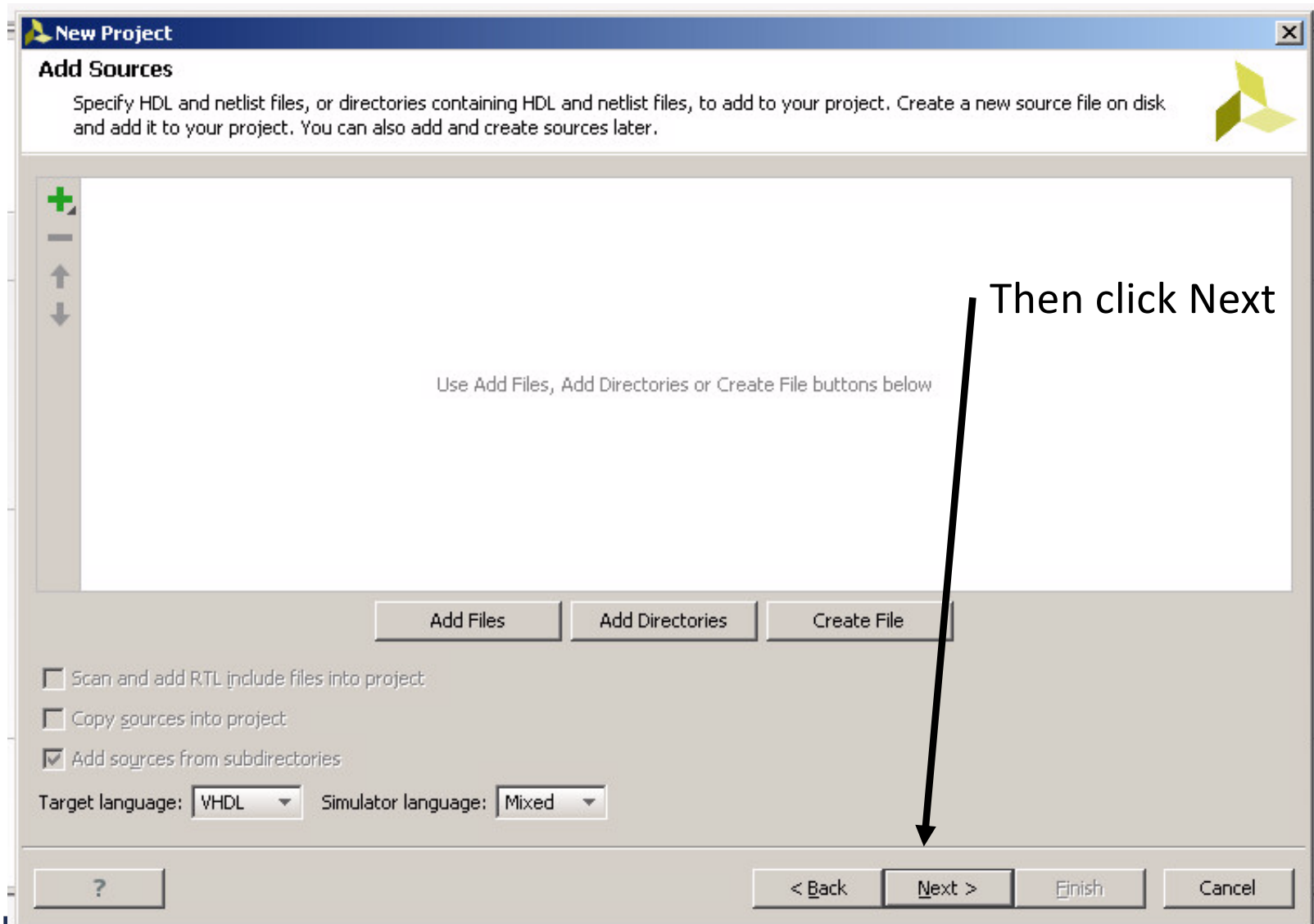
Creating Source Files



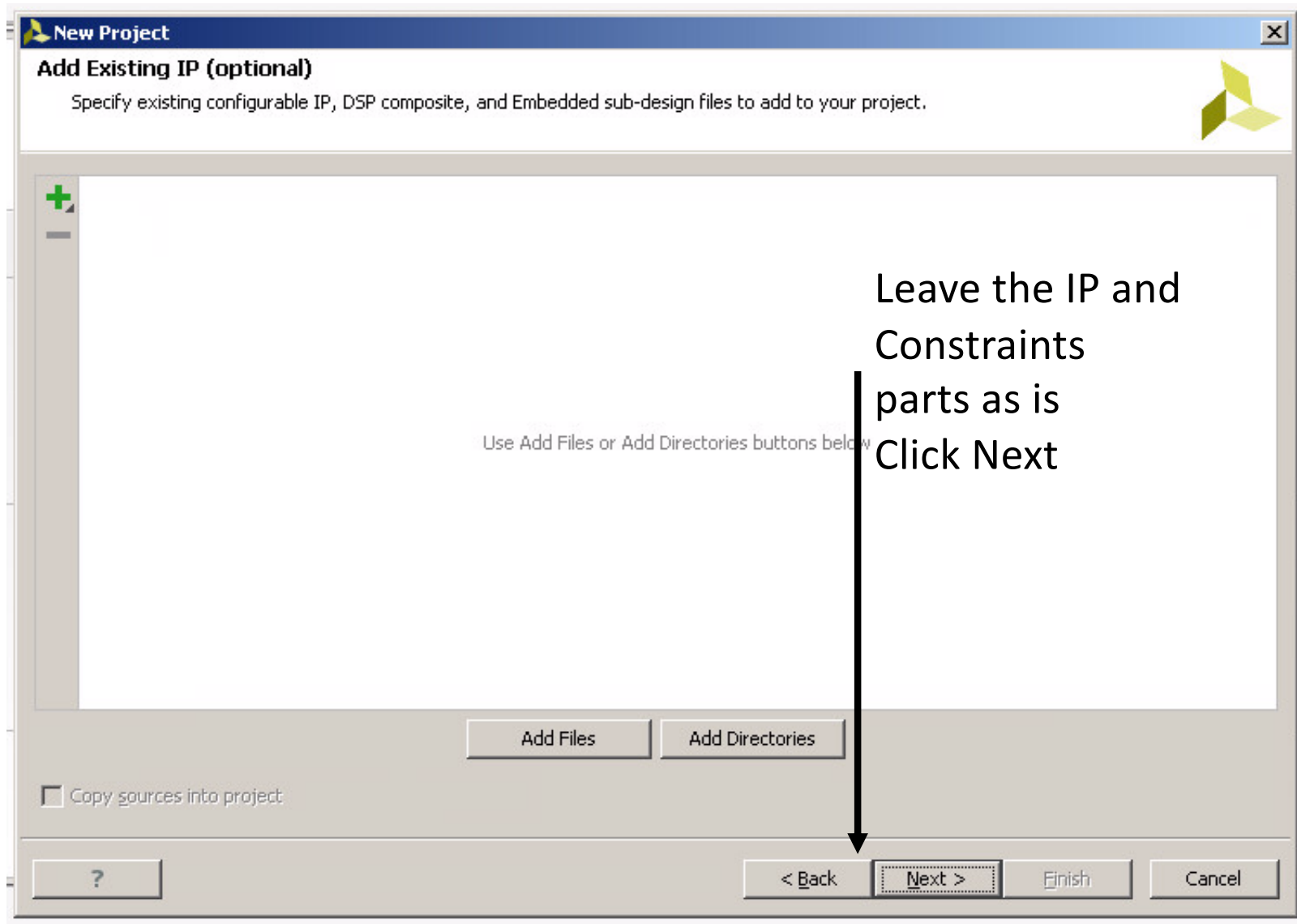
Creating Source Files



Creating Source Files



Creating Source Files



Part Selection

New Project

Default Part

Choose a default Xilinx part or board for your project. This can be changed later.

Select: Parts Boards

Filter

Product category: All Speed grade: All

Family: All Temp grade: All

Package: All

Reset All Filters

Search: Q

Part	I/O Pin Count	Block RAMs	DSPs	FlipFlops	GTPE2 Transceivers	Gb Transceivers	Available IOBs	Logic Elements
xc7k70tfbv484-1	484	135	240	82000	0	4	285	41000
xc7k70tfbv676-3	676	135	240	82000	0	8	300	41000
xc7k70tfbv676-2	676	135	240	82000	0	8	300	41000
xc7k70tfbv676-2L	676	135	240	82000	0	8	300	41000
xc7k70tfbv676-1	676	135	240	82000	0	8	300	41000
xc7k70tfbg484-2L	484	135	240	82000	0	4	285	41000
xc7k70tfbg676-2L	676	135	240	82000	0	8	300	41000
xc7k70tfbv484-2L	484	135	240	82000	0	4	285	41000
xc7k70tfbv676-2L	676	135	240	82000	0	8	300	41000
xc7k160tfn484-3	484	325	600	202800	0	4	285	101400

? < Back Next > Finish Cancel

Choose the default FPGA
xc7k70tfbv676-1
Then click next
Then click finish
The project will then
be created

Port Definitions

Leave this part as is and click OK
You will be adding the port definitions in the VHDL code later

Define a module and specify I/O Ports to add to your source file.
For each port specified:
MSB and LSB values will be ignored unless its Bus column is checked.
Ports with blank names will not be written.

Module Definition

Entity name: lab0

Architecture name: Behavioral

I/O Port Definitions

	Port Name	Direction	Bus	MSB	LSB
+		in	<input type="checkbox"/>	0	0
-					
↑					
↓					

?

OK Cancel

Start Programming

1. Double-click on 'lab0 – Behavioral' for the lab0.vhd file to open in the right panel

```
1  -- Simulation Tutorial
2  -- 1-bit Adder
3
4  -- This is just to make a referenc
5  LIBRARY IEEE;
6  use IEEE.STD_LOGIC_1164.ALL;
7  use IEEE.NUMERIC_STD.ALL;
8
9  -- We declare the 1-bit adder with
10 -- shown inside the port().
```

2. Copy & Paste the code from lab0.vhd here (It is a 1-bit adder that is downloadable from the course webpage). Save lab0.vhd using Ctrl+S. The left panel should now say BIT_ADDER – BHV under Design Sources

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Failed Routes	LUT	FF	B
synth_1	constrs_1	Not started									
impl_1	constrs_1	Not started									

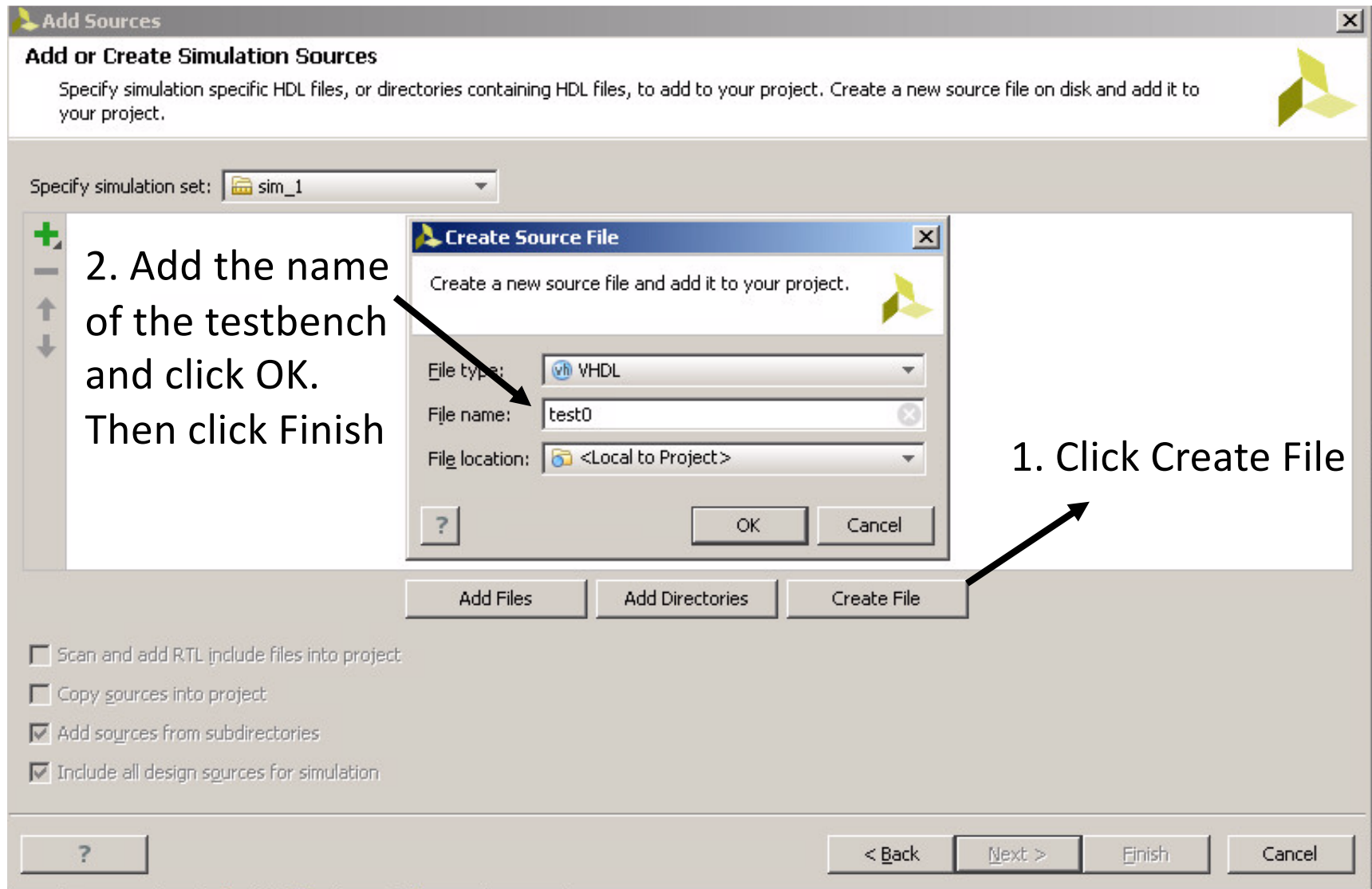
Adding a Test Bench

1. Click here to add a new file

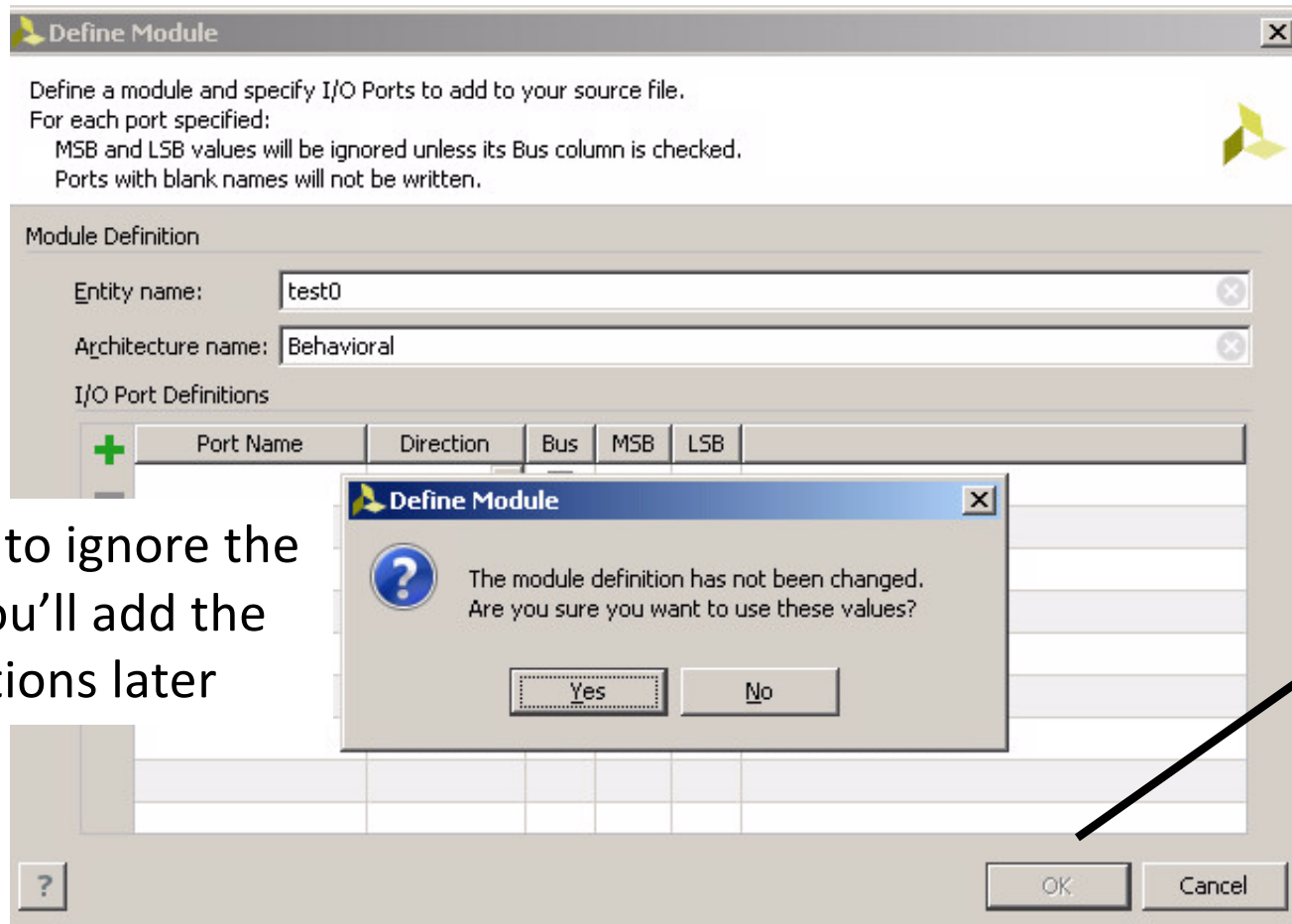
2. Select Simulation Sources here and click Next

Specify and/or create source files to add to the project

Adding a Test Bench



Adding a Test Bench



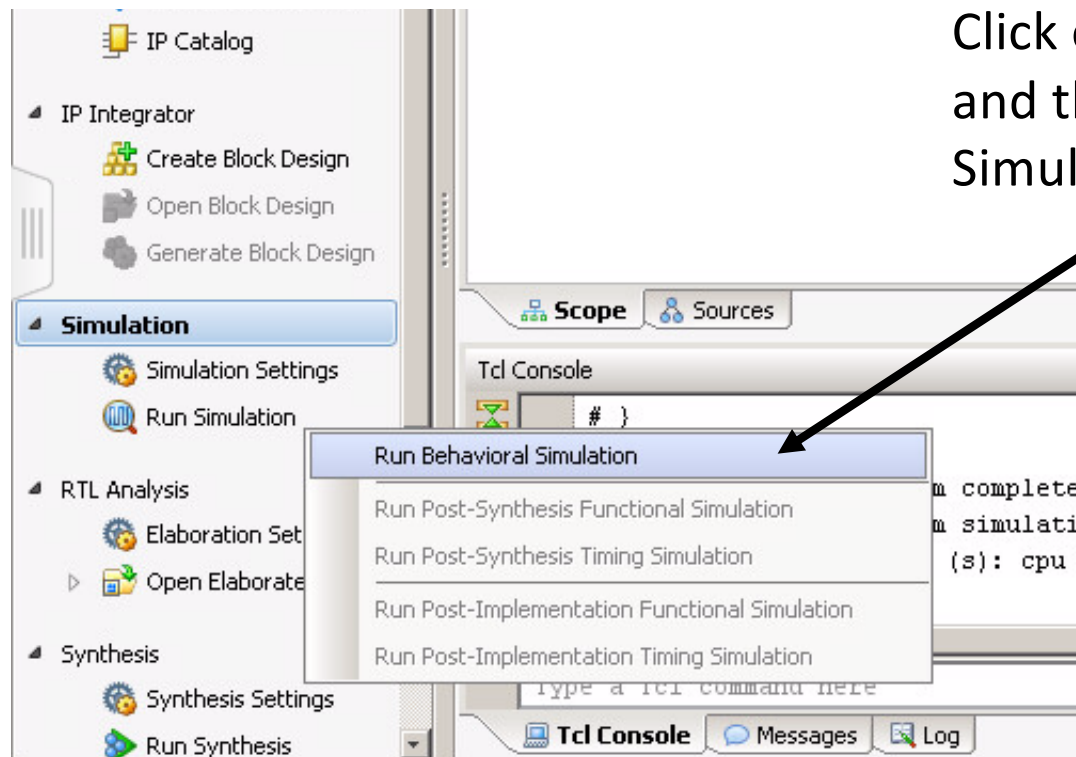
Copy the testbench Code

1. Click Simulation Sources then sim_1, and then double-click on 'test0 - Behavioral' for the test0.vhd file to open in the right panel

```
15 -- input or output ports.  
16 entity TEST_ADD is  
17  
18  
19  
20  
21  
22  
23  
24
```

2. Copy & Paste the code from test0.vhd here (It is a 1-bit adder that is downloadable from the course webpage). Save test0.vhd using Ctrl+S. The left panel should now say TEST_ADD – TEST under Simulation Sources and sim_1

Running Simulation



Click on Run Simulation,
and then Run Behavioral
Simulation

Behavioral Simulation

- A waveform window should automatically open after you click Run Simulation
- Enables one to visualize waveforms for the digital design
 - Runs for the time specified in the test bench
 - Allows one to visualize interface as well as internal state of the simulated design
 - Simulates input configurations specified in the test bench

Running the Simulation

The screenshot shows a behavioral simulation window titled "Behavioral Simulation - Functional - sim_1 - TEST_ADD". The interface includes a Project Manager on the left, a Scope panel, and a main simulation area. The Scope panel lists signals: A[0:0], B[0:0], CIN[0:0], SUM, and COUT. A "Zoom Fit" button is visible. The main area displays a table of signal values and a timing diagram on the right.

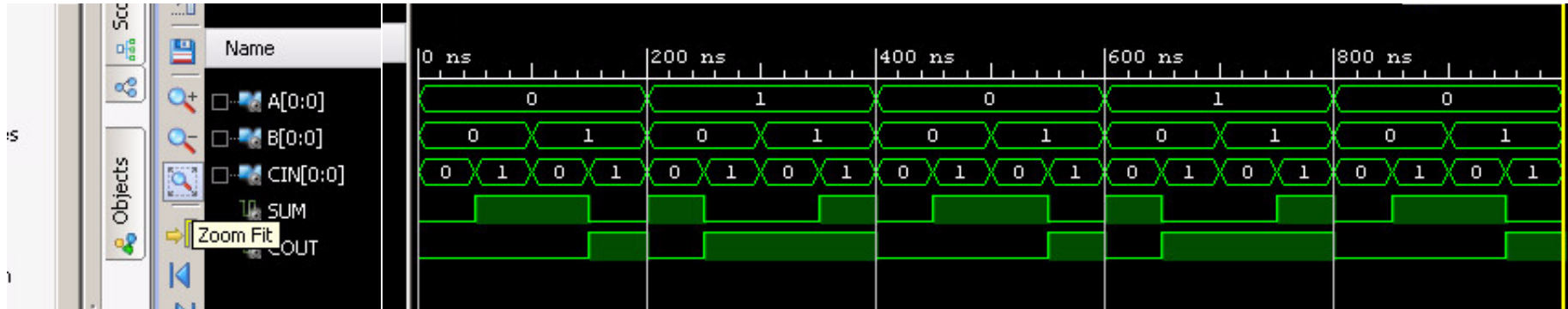
Name	Value
A[0:0]	1
B[0:0]	0
CIN[0:0]	0
SUM	1
COUT	0

The timing diagram on the right shows waveforms for signals A, B, CIN, SUM, and COUT over a time range from 0 ns to 200 ns. The signals are represented by green waveforms on a black background.

Click to Zoom Fit

These interface signals should automatically appear

Check Waveform



- You should study lab0.vhd code and then understand how test0.vhd sensitizes inputs to create a testbench to test the 1-bit adder circuit
- The SUM and COUT outputs can be verified by visually inspecting the A, B and CIN inputs at various timestamps