PA0 Guide

ECE 3401 – Spring 2021

Course TA contact information:

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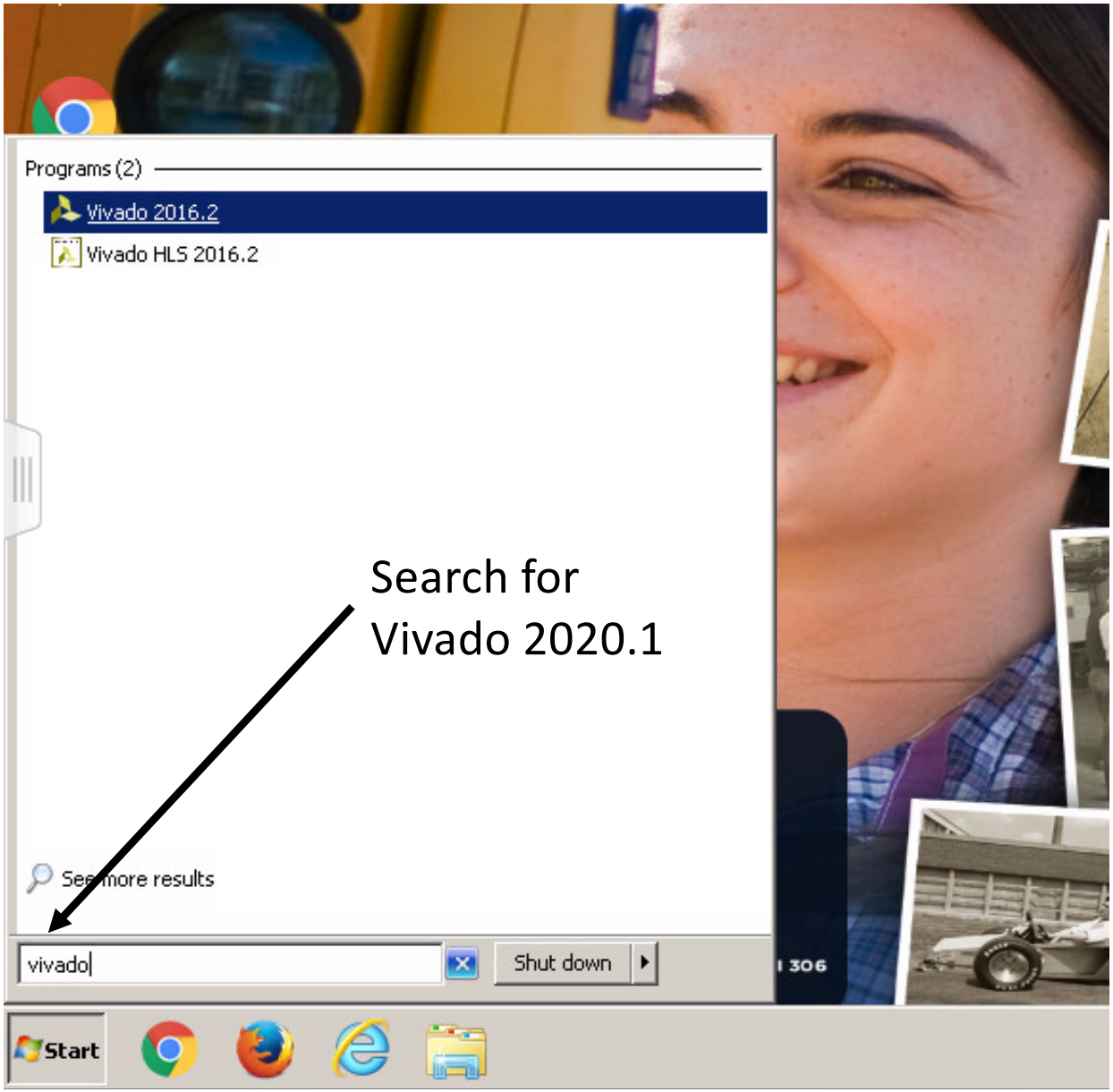
UCONN

UConn AnyWare Login Steps

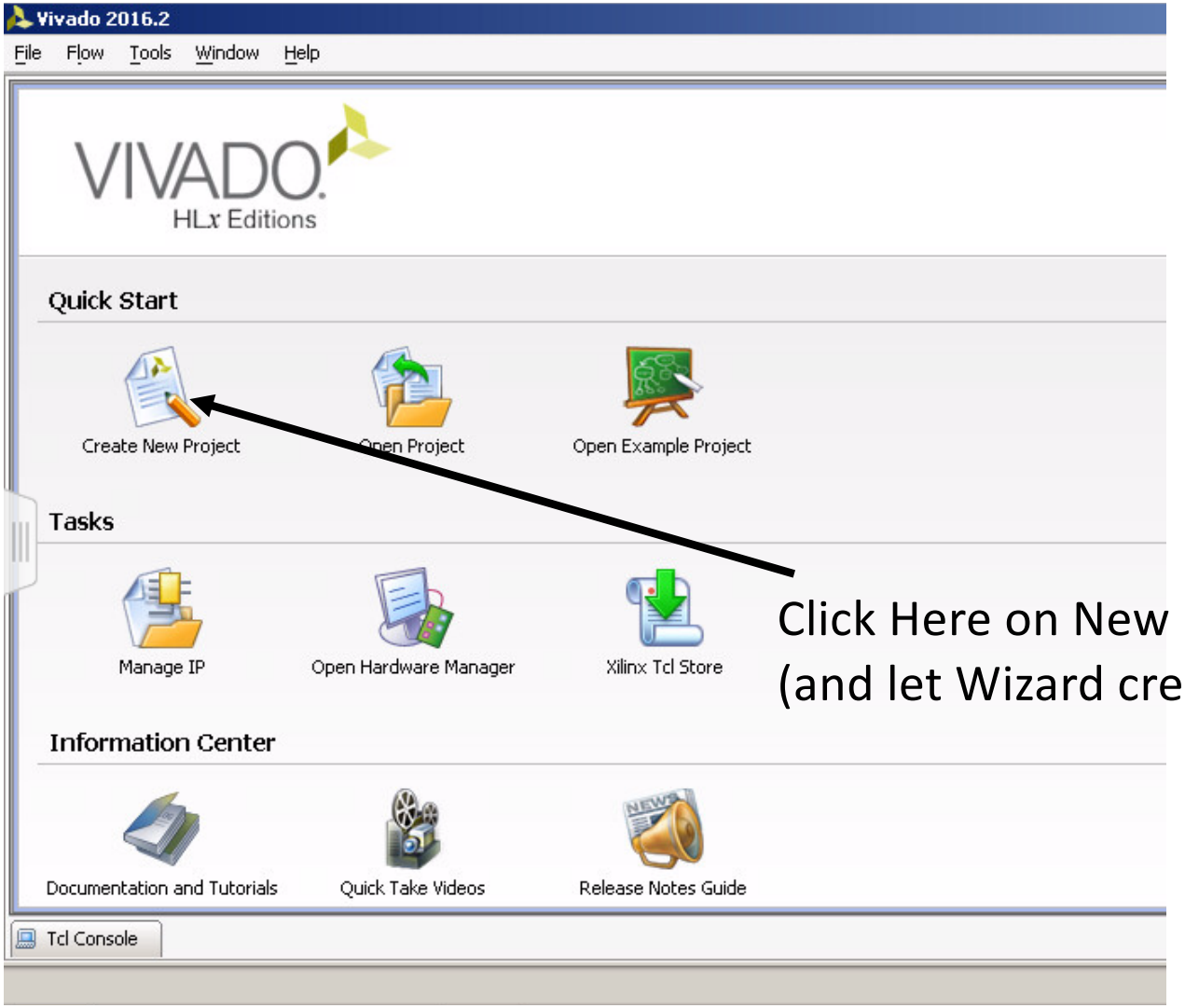
1. Open https://software.uconn.edu/uconn-software-online/
2. Click on the “Launch school specific desktops” icon under Launch AnyWare
3. Under the VMware Horizon: Enter your NetID as Username, and enter your password
4. When you login, you will be using “Engineering Desktop”. Click on the “Engineering Desktop”, and wait for you to get logged into the VM
5. On the left Window menu, select “Xilinx” at the end of the menu
6. Within Xilinx, click on “Vivado 2020.1” and wait for the tool to open

UCONN

Start Vivado



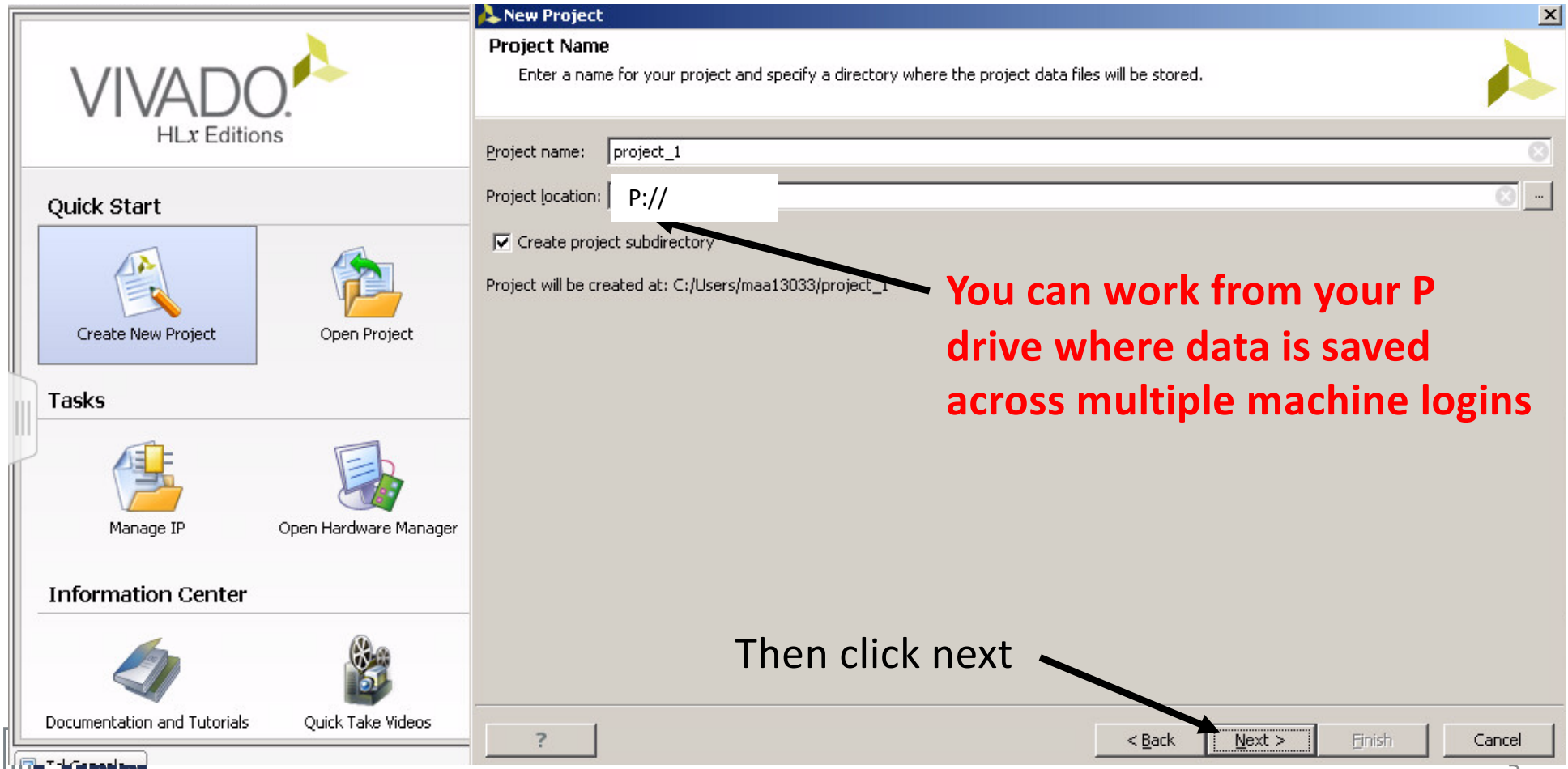
Create a New Project



Click Here on New Project
(and let Wizard create a new project)

Project Wizard

- The project wizard will open. Give any name to your project (e.g. lab0) and leave the rest as is



Project Wizard

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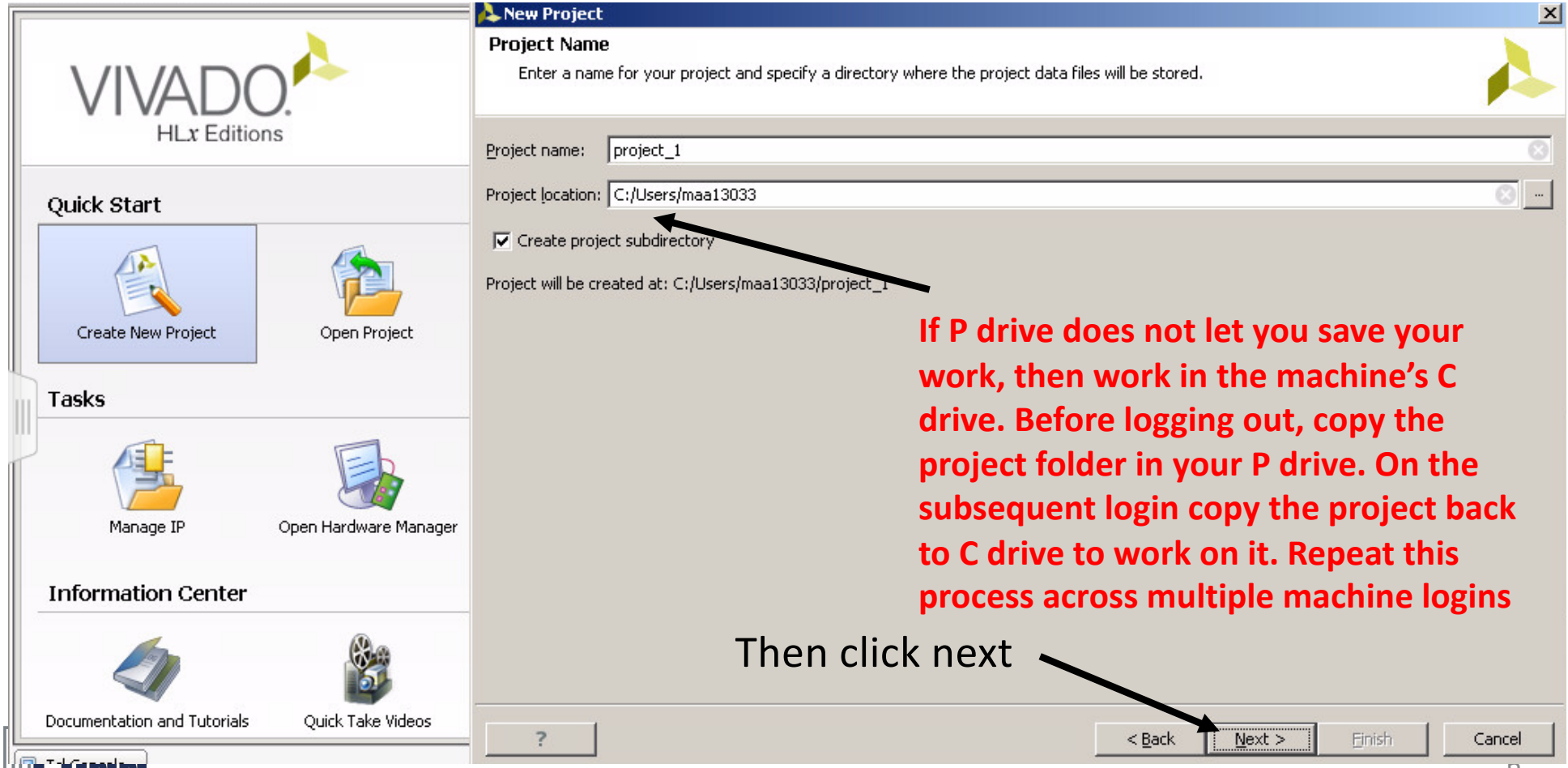
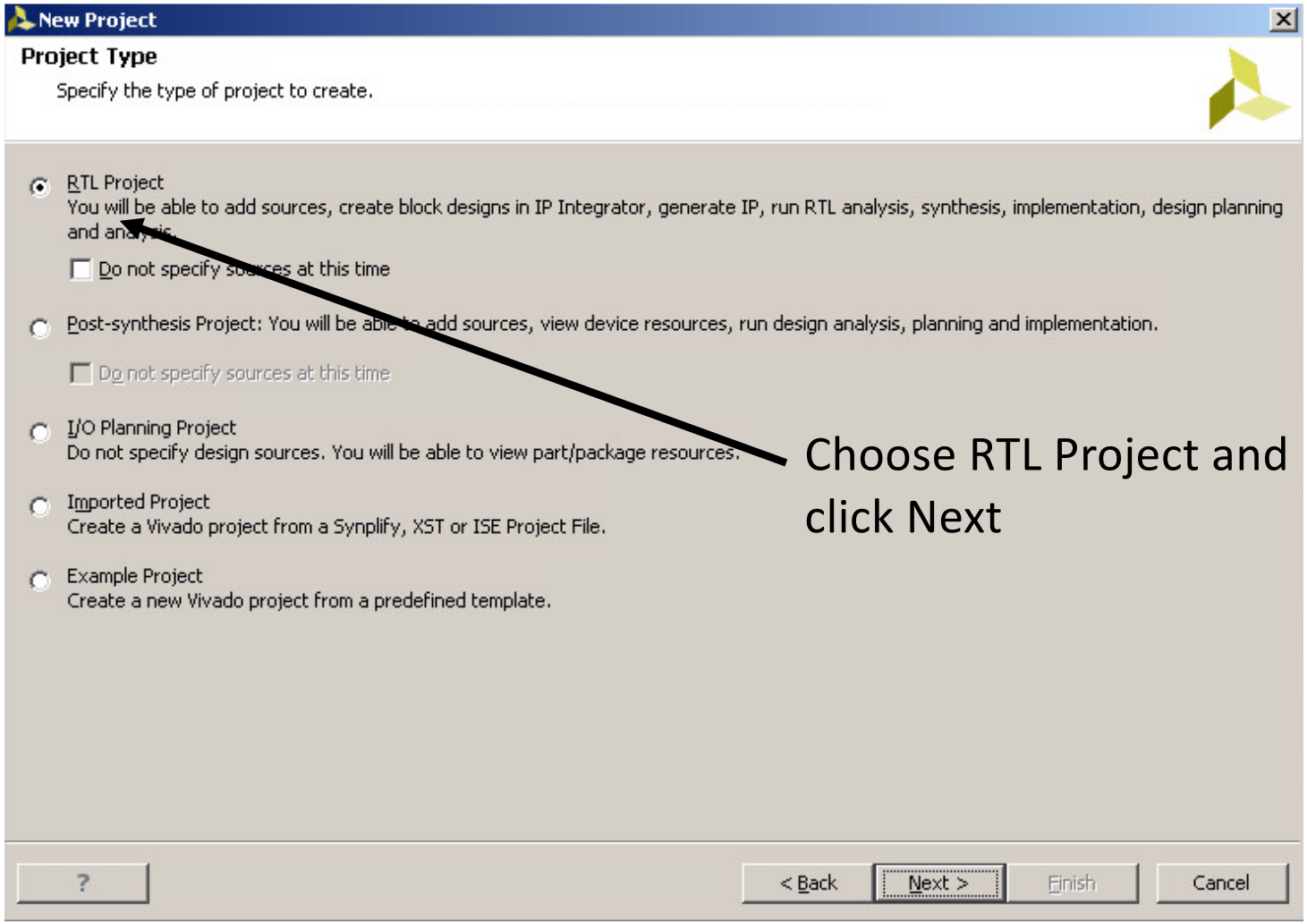
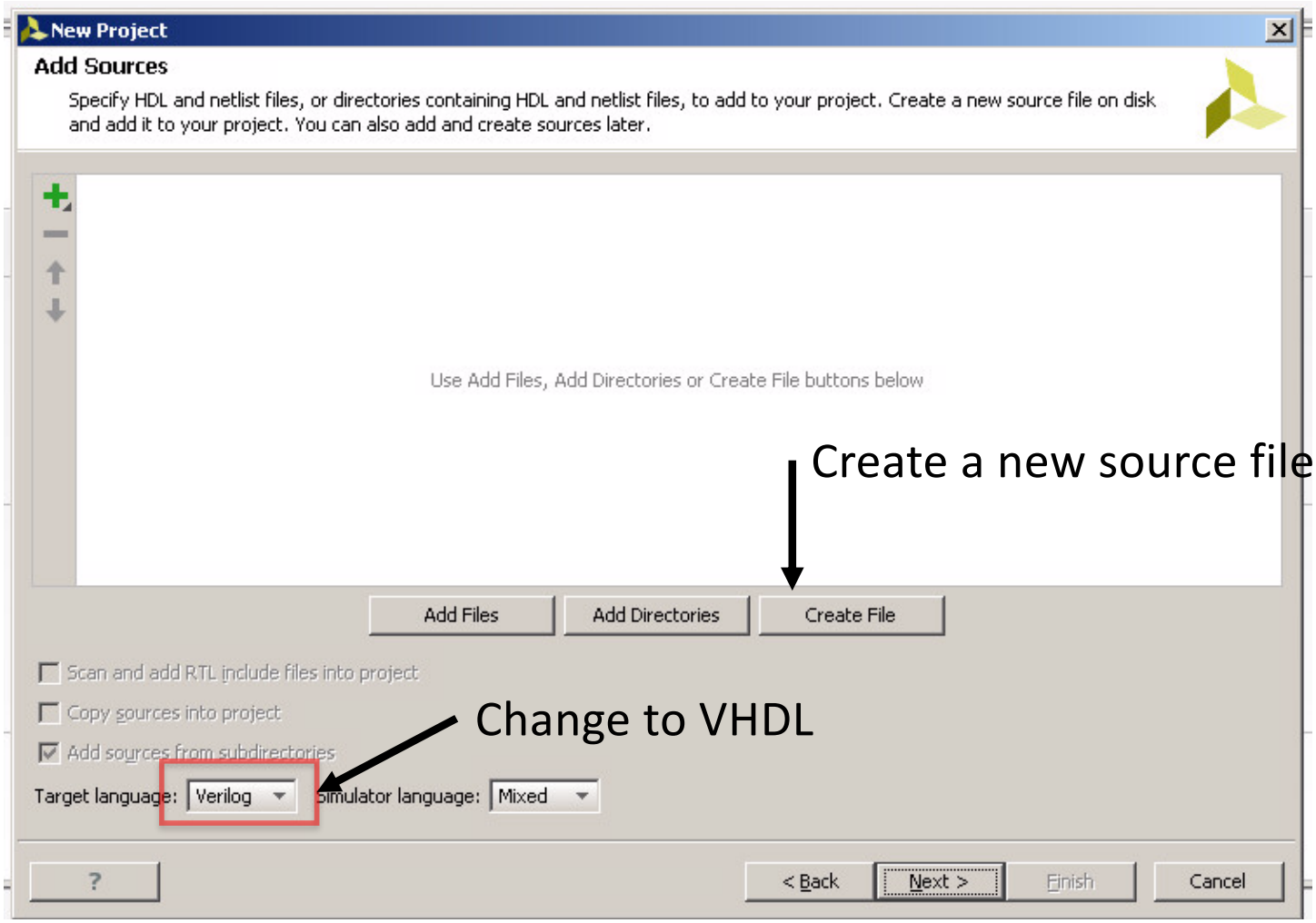


Project Settings

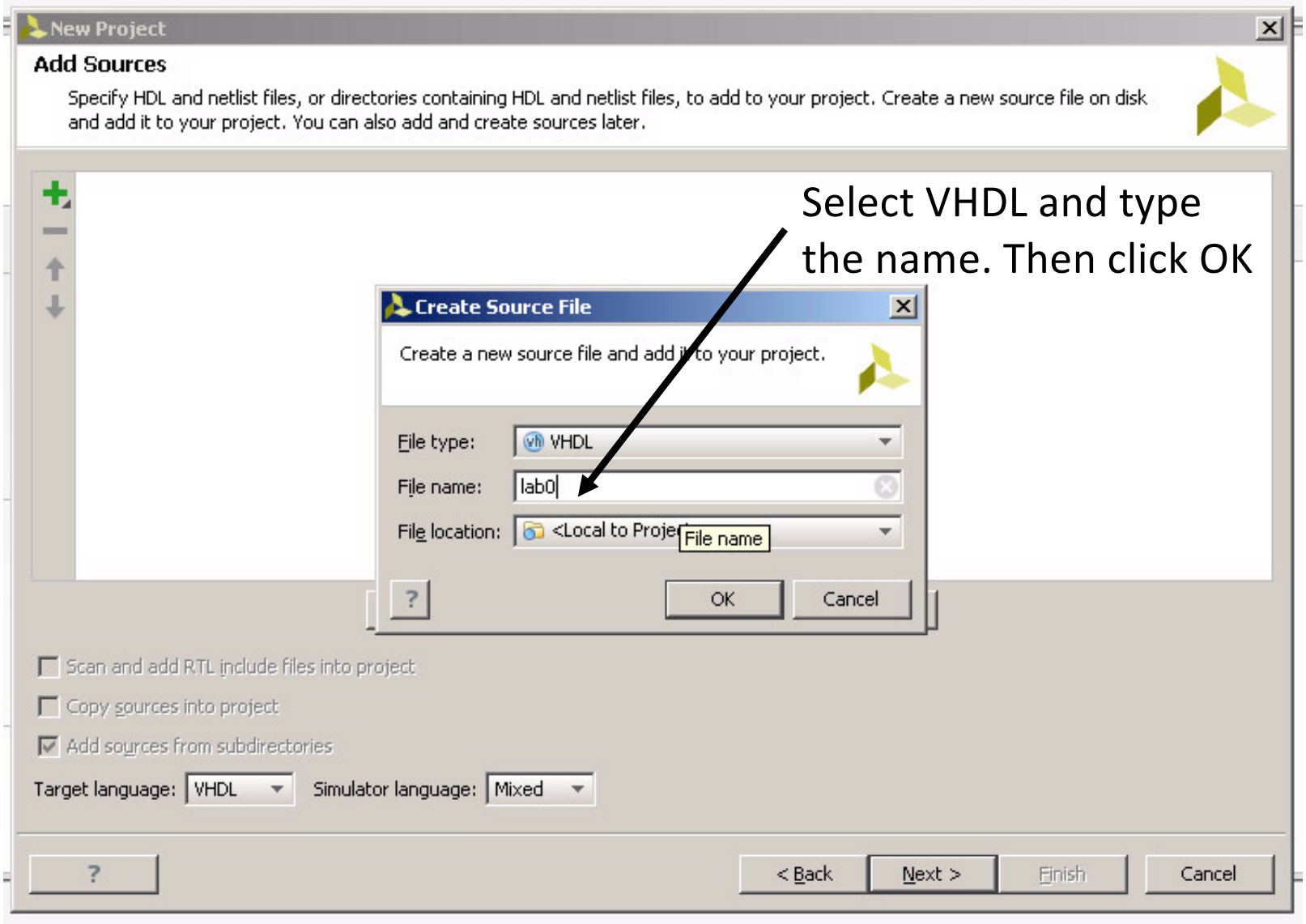
- Select RTL Project, then click next
- And then Finish



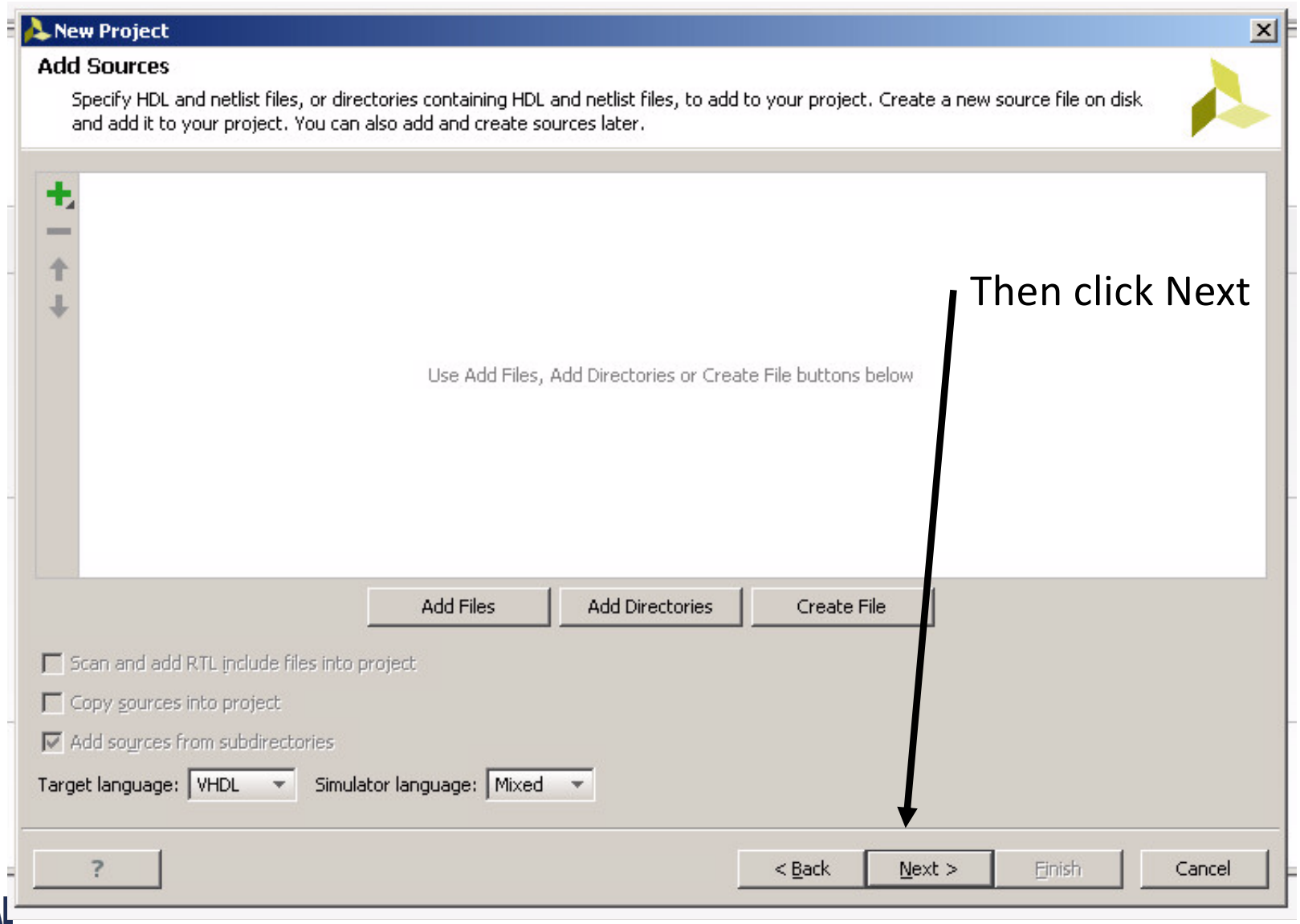
Creating Source Files



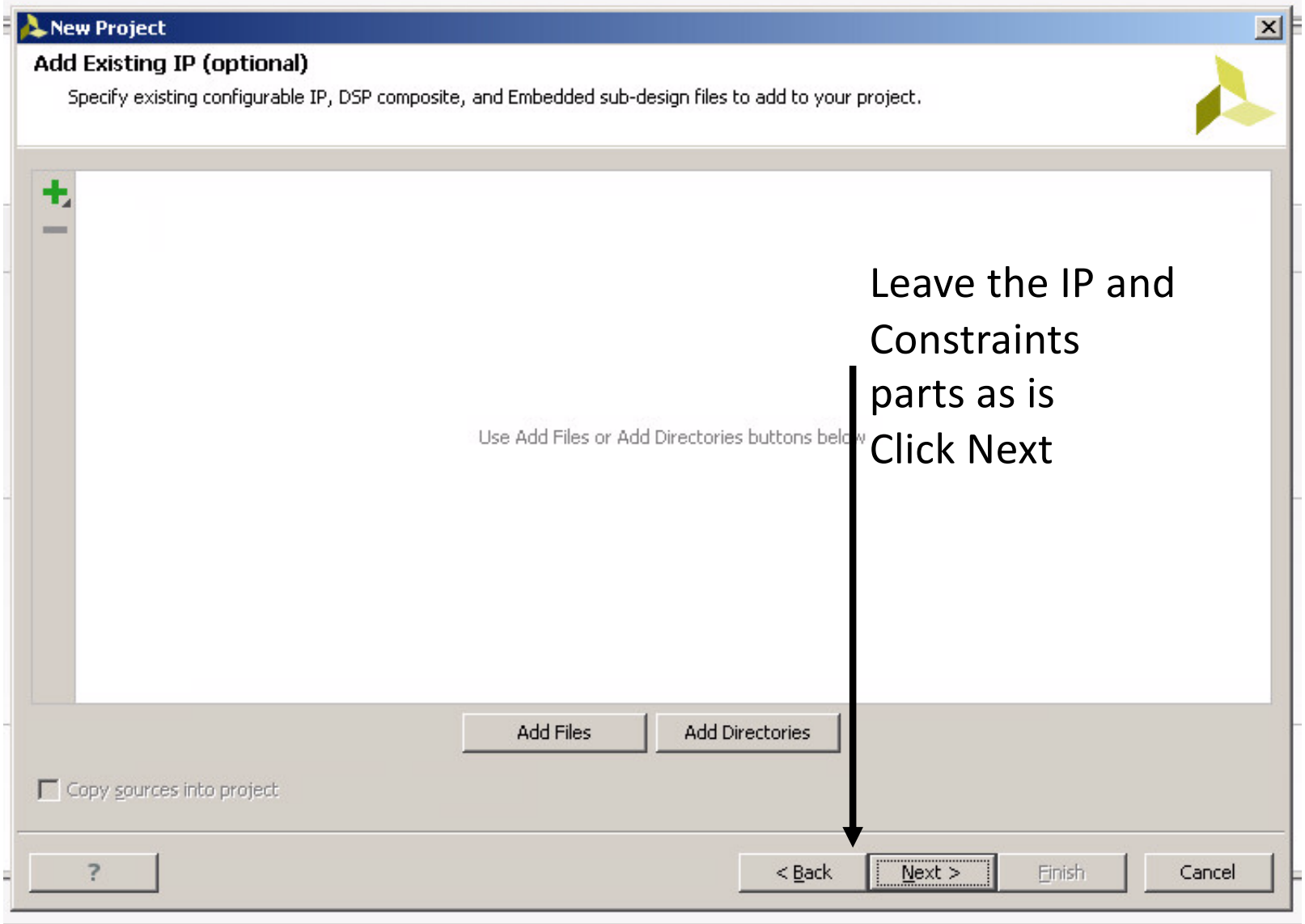
Creating Source Files



Creating Source Files

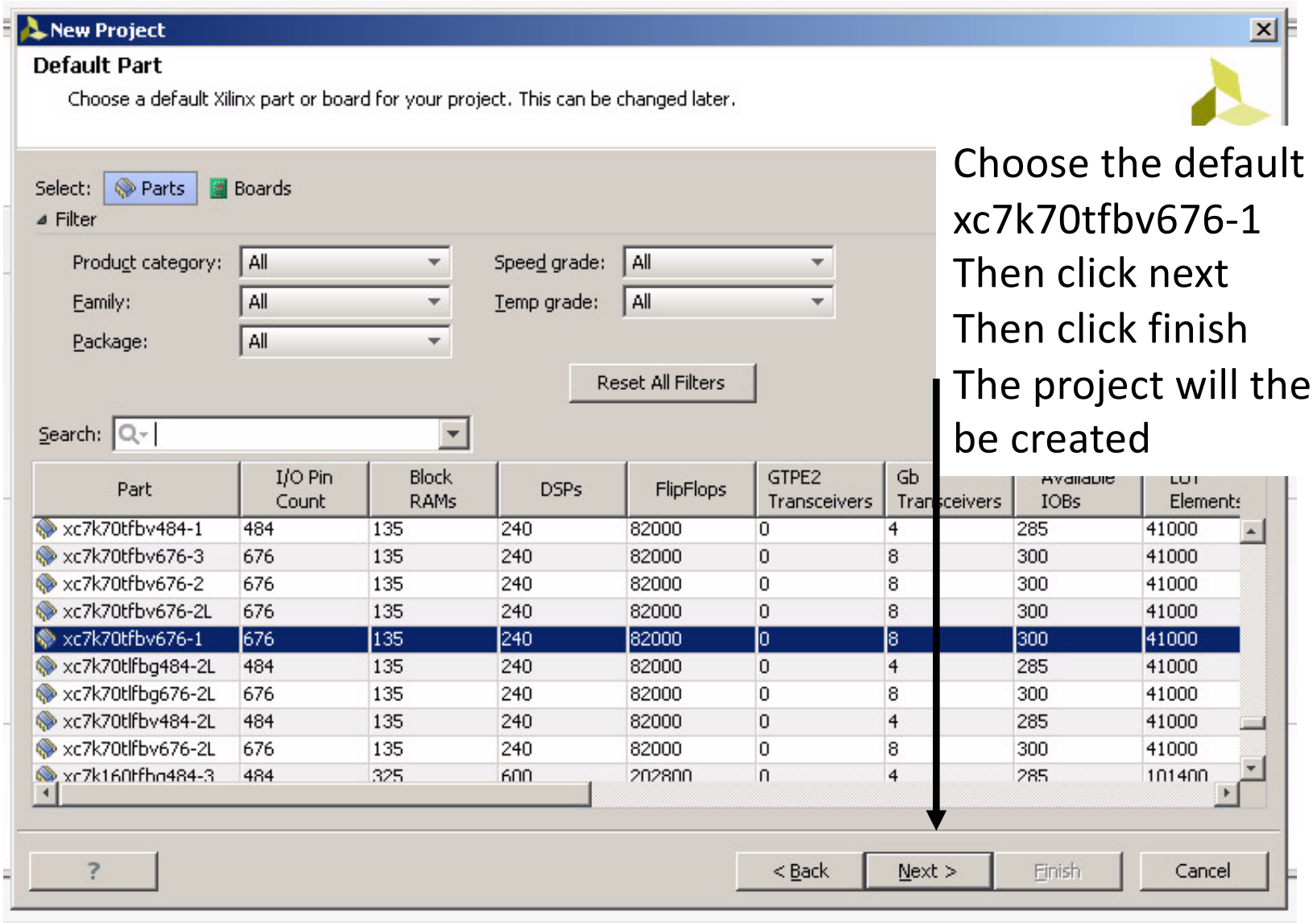


Creating Source Files



Leave the IP and Constraints parts as is
Click Next

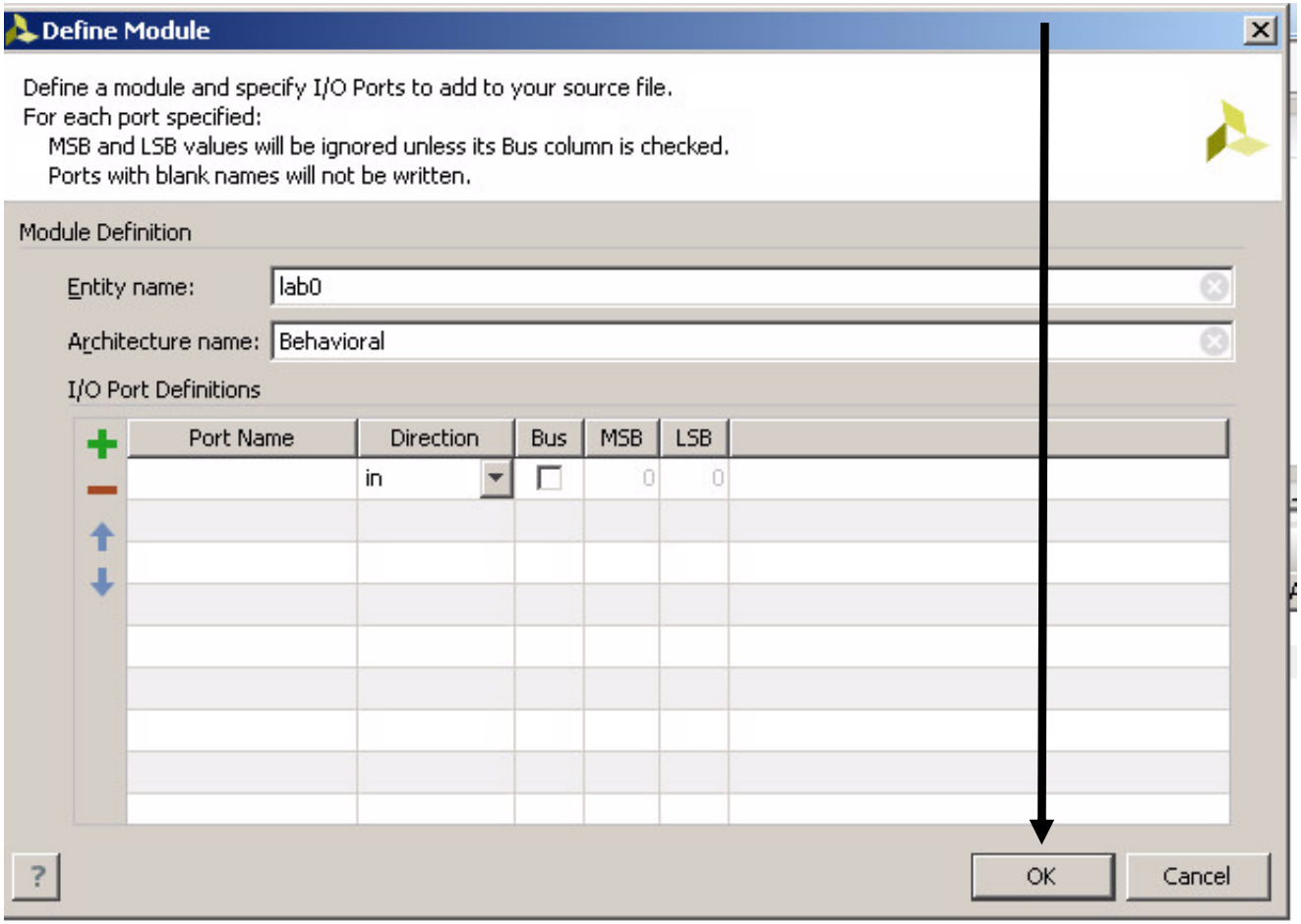
Part Selection



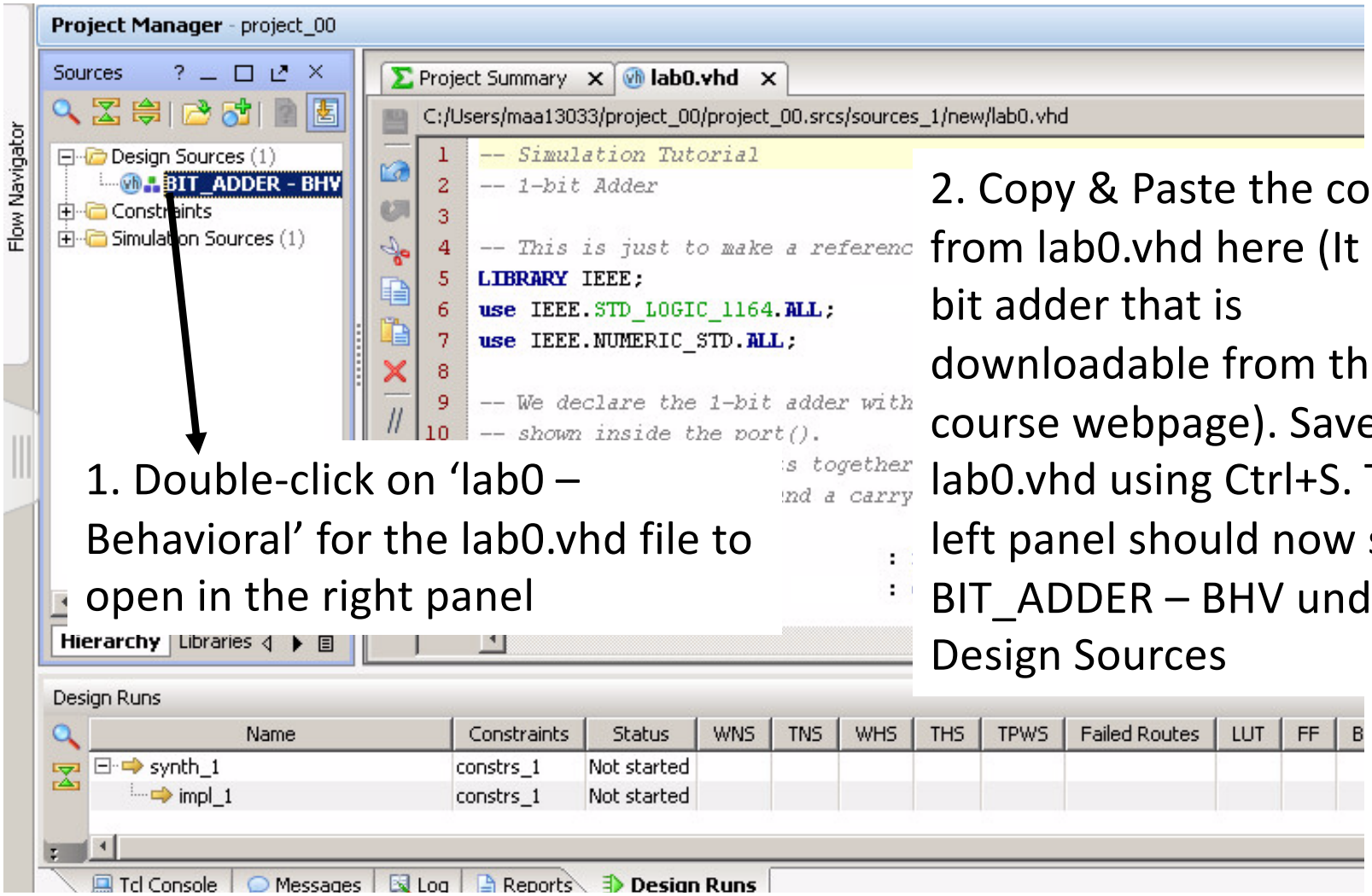
Choose the default FPGA xc7k70tfbv676-1
Then click next
Then click finish
The project will then be created

Port Definitions

Leave this part as is and click OK
You will be adding the port definitions in the VHDL code later



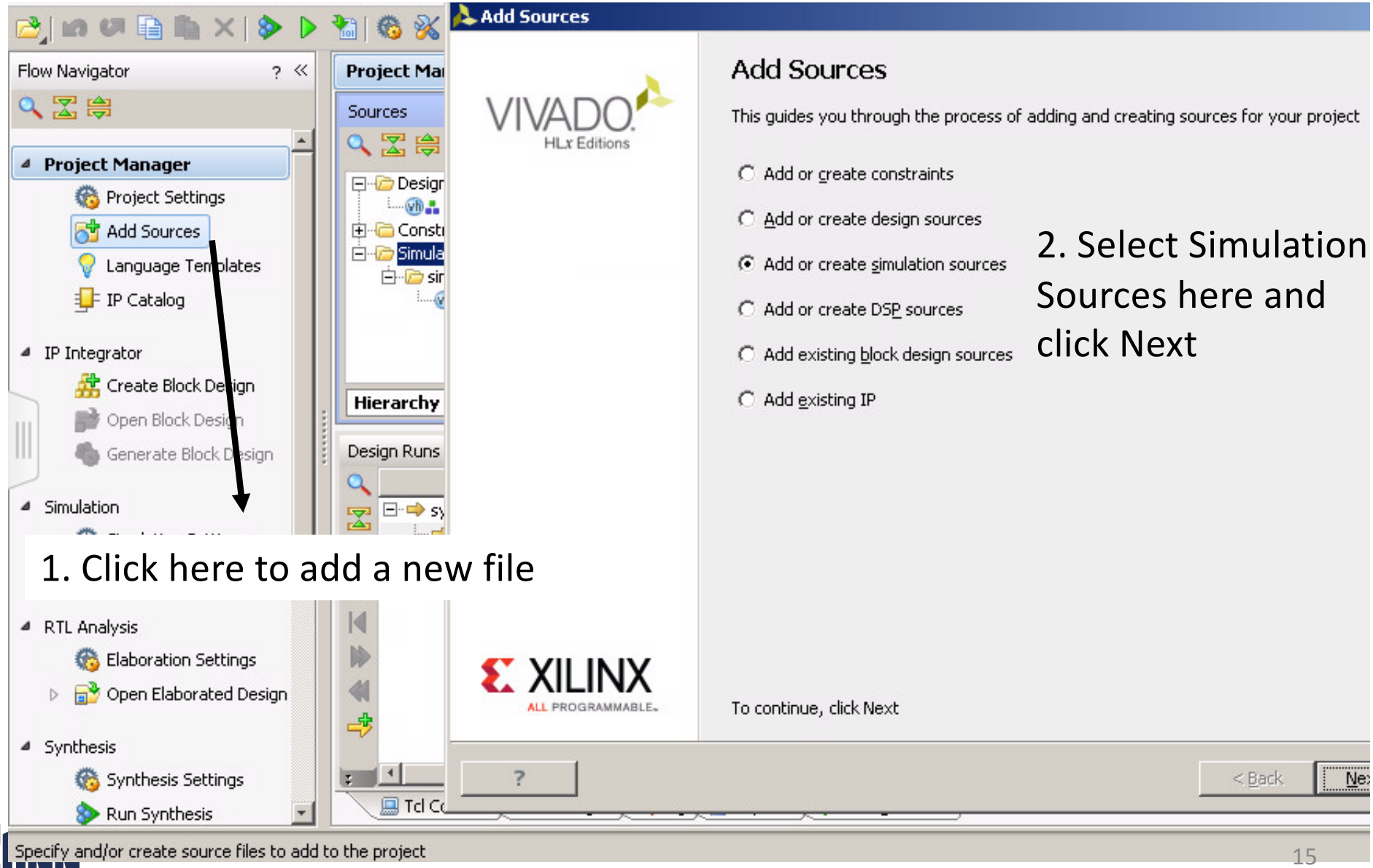
Start Programming



1. Double-click on 'lab0 – Behavioral' for the lab0.vhd file to open in the right panel

2. Copy & Paste the code from lab0.vhd here (It is a 1-bit adder that is downloadable from the course webpage). Save lab0.vhd using Ctrl+S. The left panel should now say BIT_ADDER – BHV under Design Sources

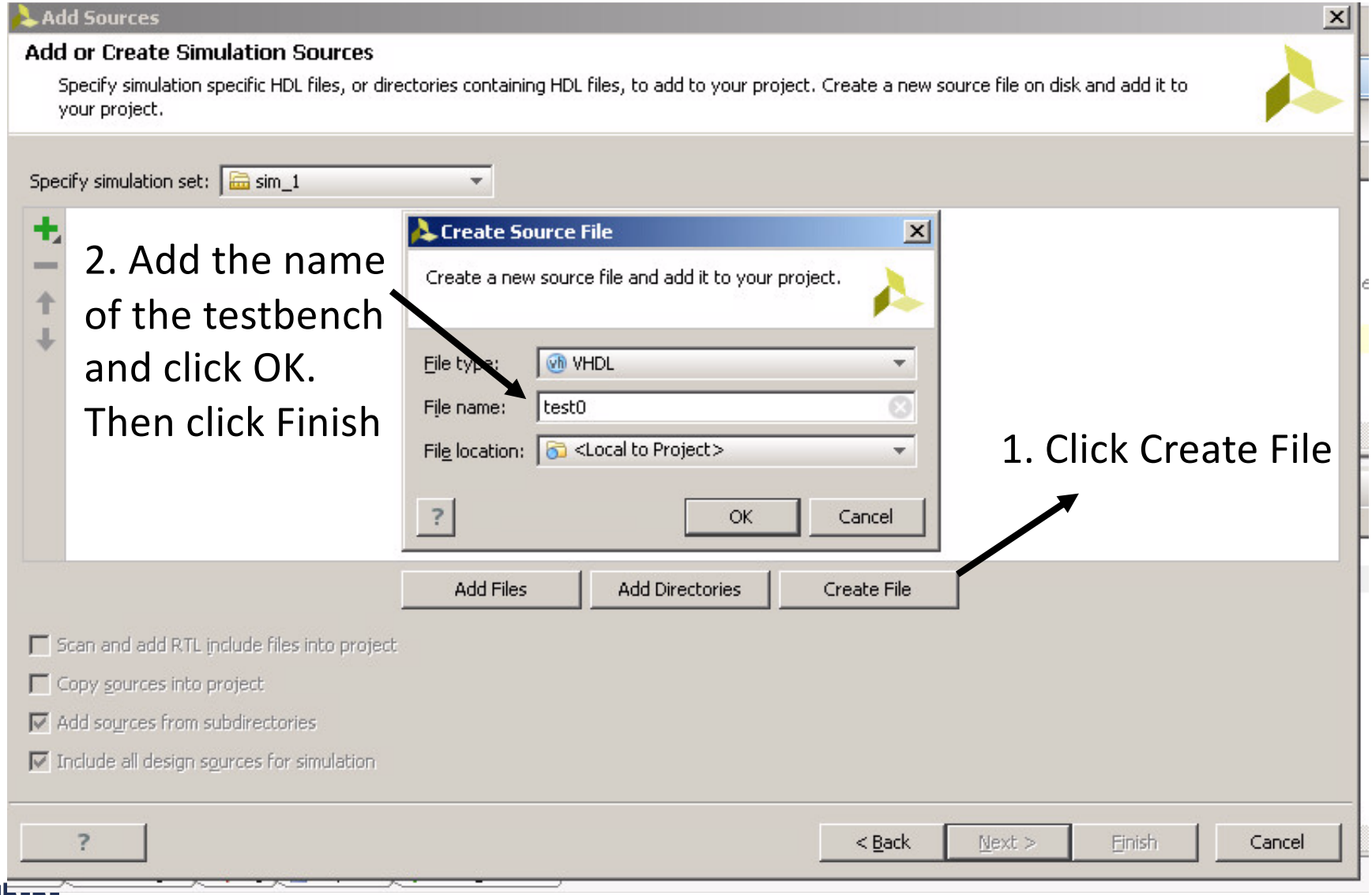
Adding a Test Bench



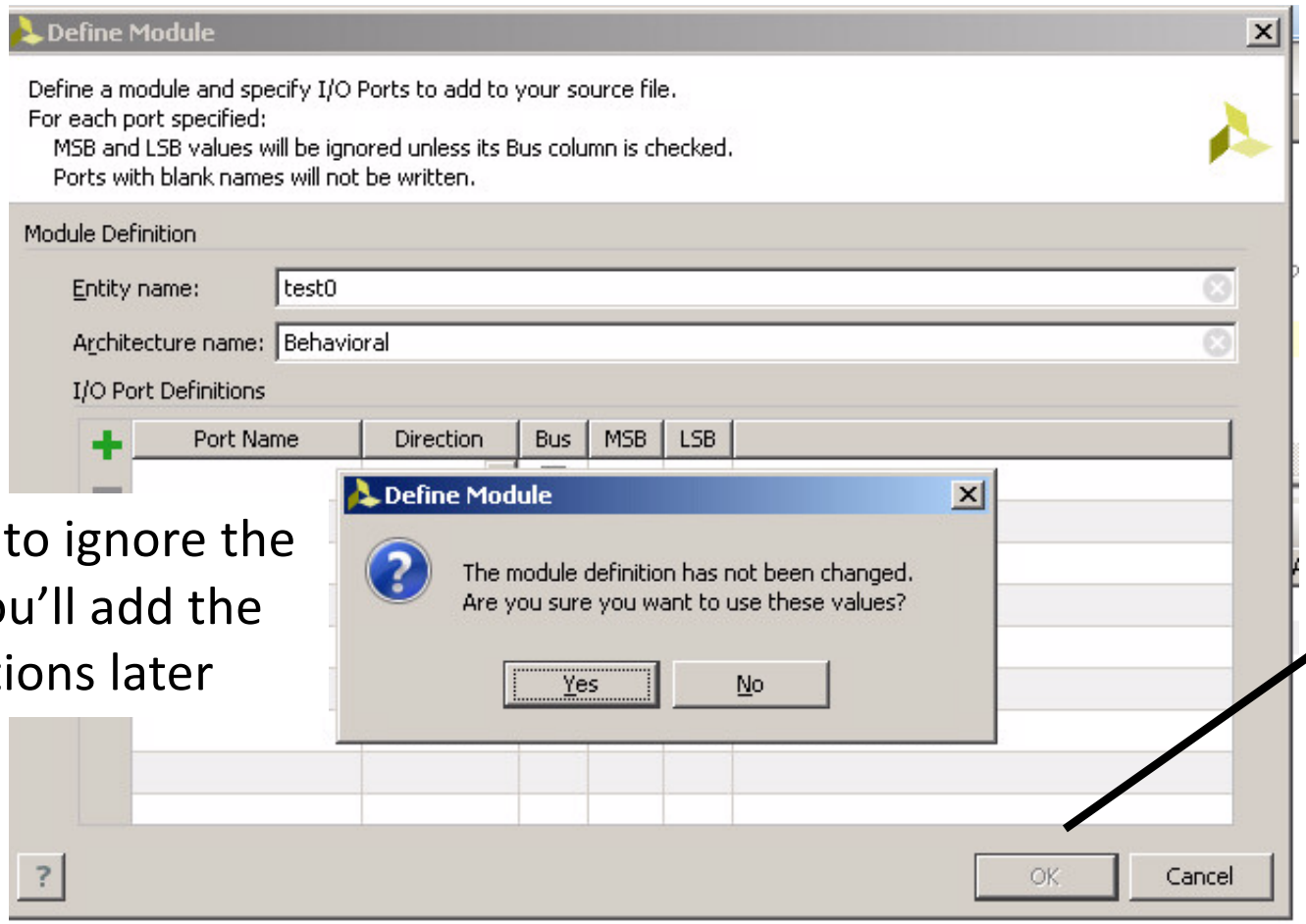
1. Click here to add a new file

2. Select Simulation Sources here and click Next

Adding a Test Bench



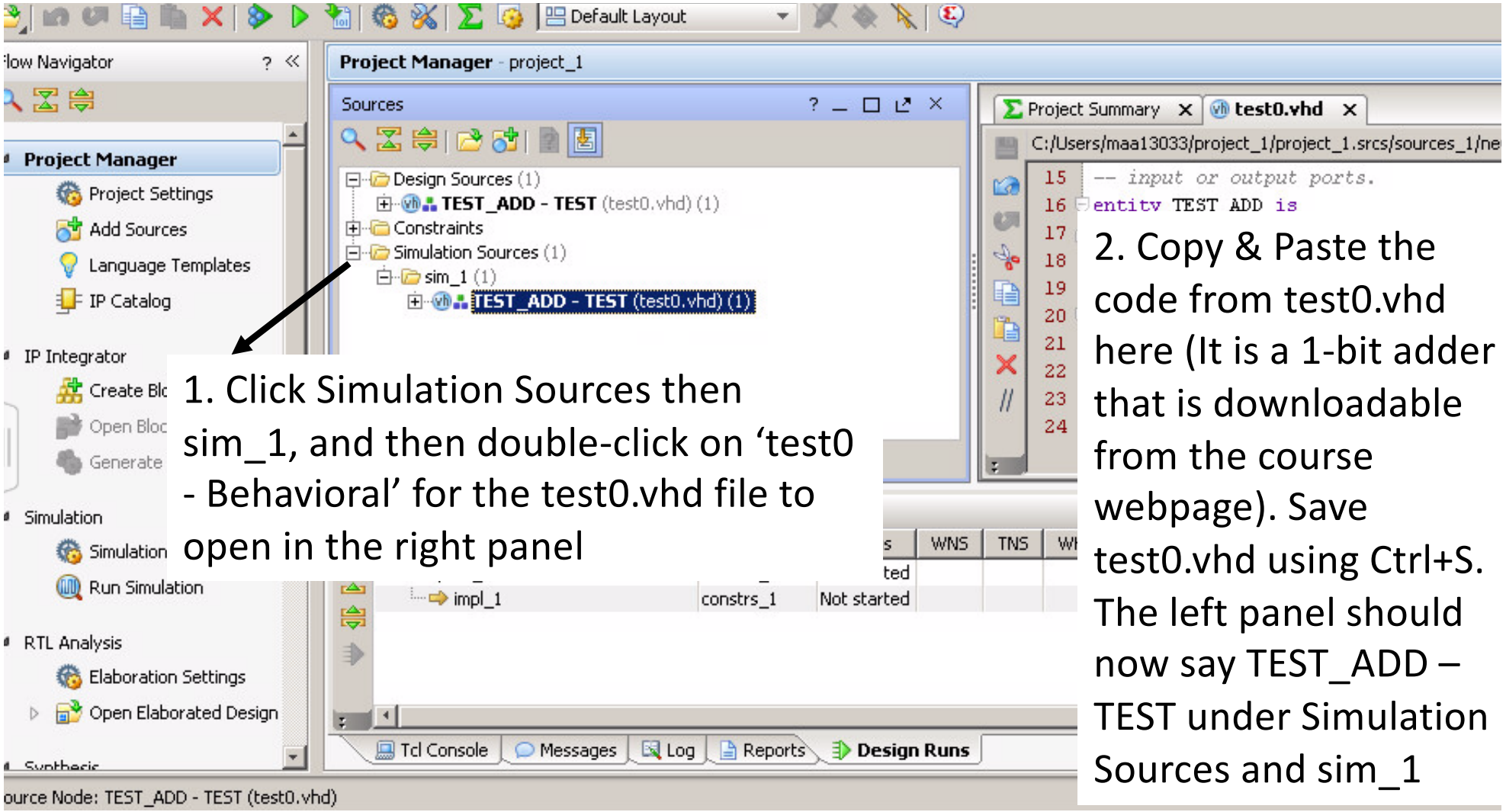
Adding a Test Bench



2. Click Yes to ignore the warning. You'll add the port definitions later

1. Click OK

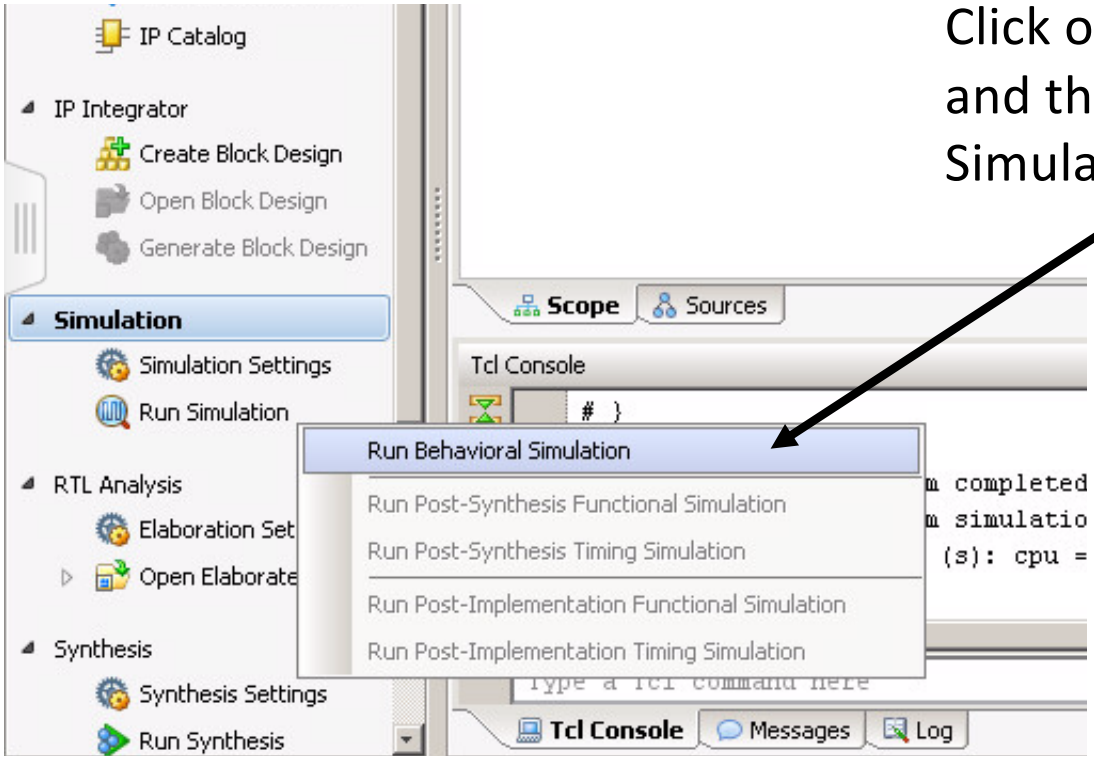
Copy the testbench Code



1. Click Simulation Sources then sim_1, and then double-click on 'test0 - Behavioral' for the test0.vhd file to open in the right panel

2. Copy & Paste the code from test0.vhd here (It is a 1-bit adder that is downloadable from the course webpage). Save test0.vhd using Ctrl+S. The left panel should now say TEST_ADD – TEST under Simulation Sources and sim_1

Running Simulation

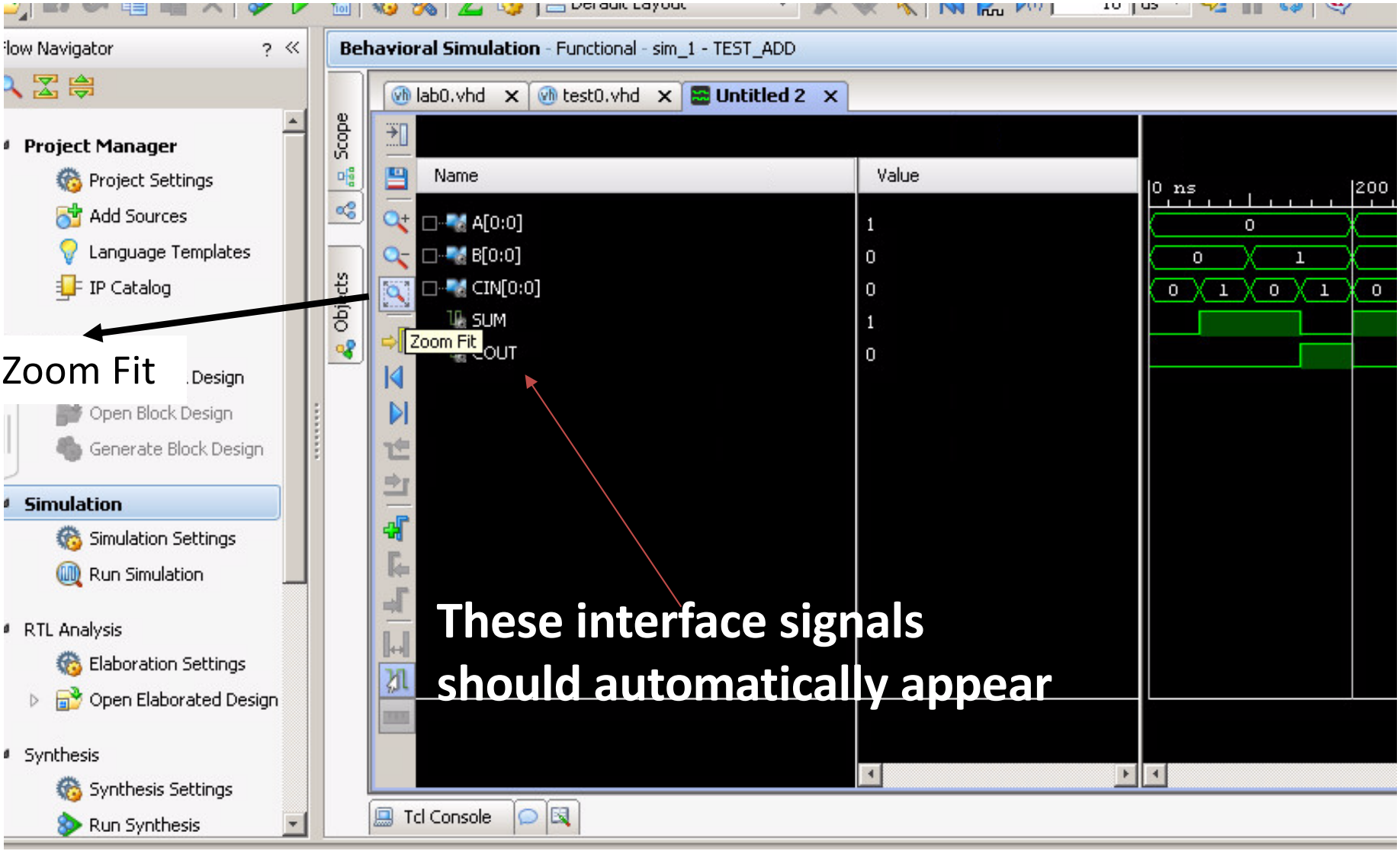


Click on Run Simulation, and then Run Behavioral Simulation

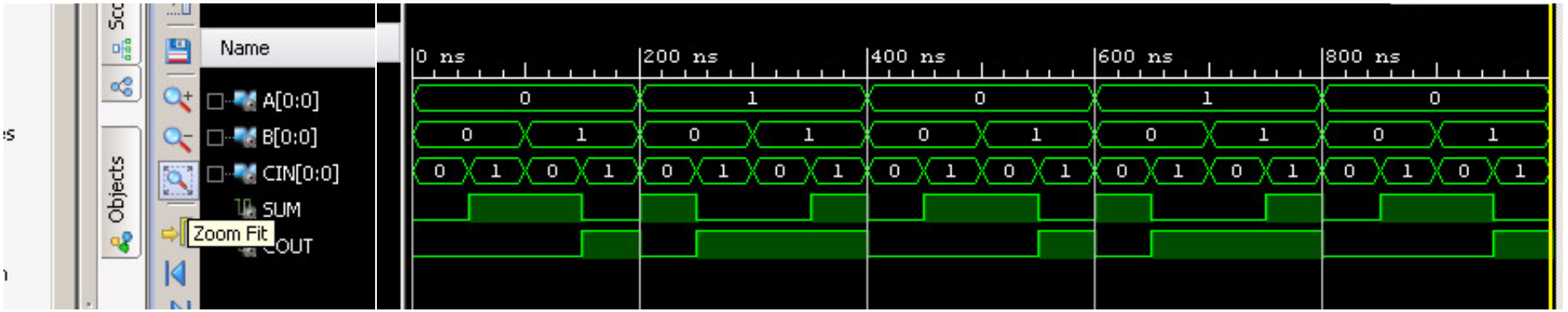
Behavioral Simulation

- A waveform window should automatically open after you click Run Simulation
- Enables one to visualize waveforms for the digital design
  - Runs for the time specified in the test bench
  - Allows one to visualize interface as well as internal state of the simulated design
  - Simulates input configurations specified in the test bench

Running the Simulation



Check Waveform



- You should study lab0.vhd code and then understand how test0.vhd sensitizes inputs to create a testbench to test the 1-bit adder circuit
- The SUM and COUT outputs can be verified by visually inspecting the A, B and CIN inputs at various timestamps