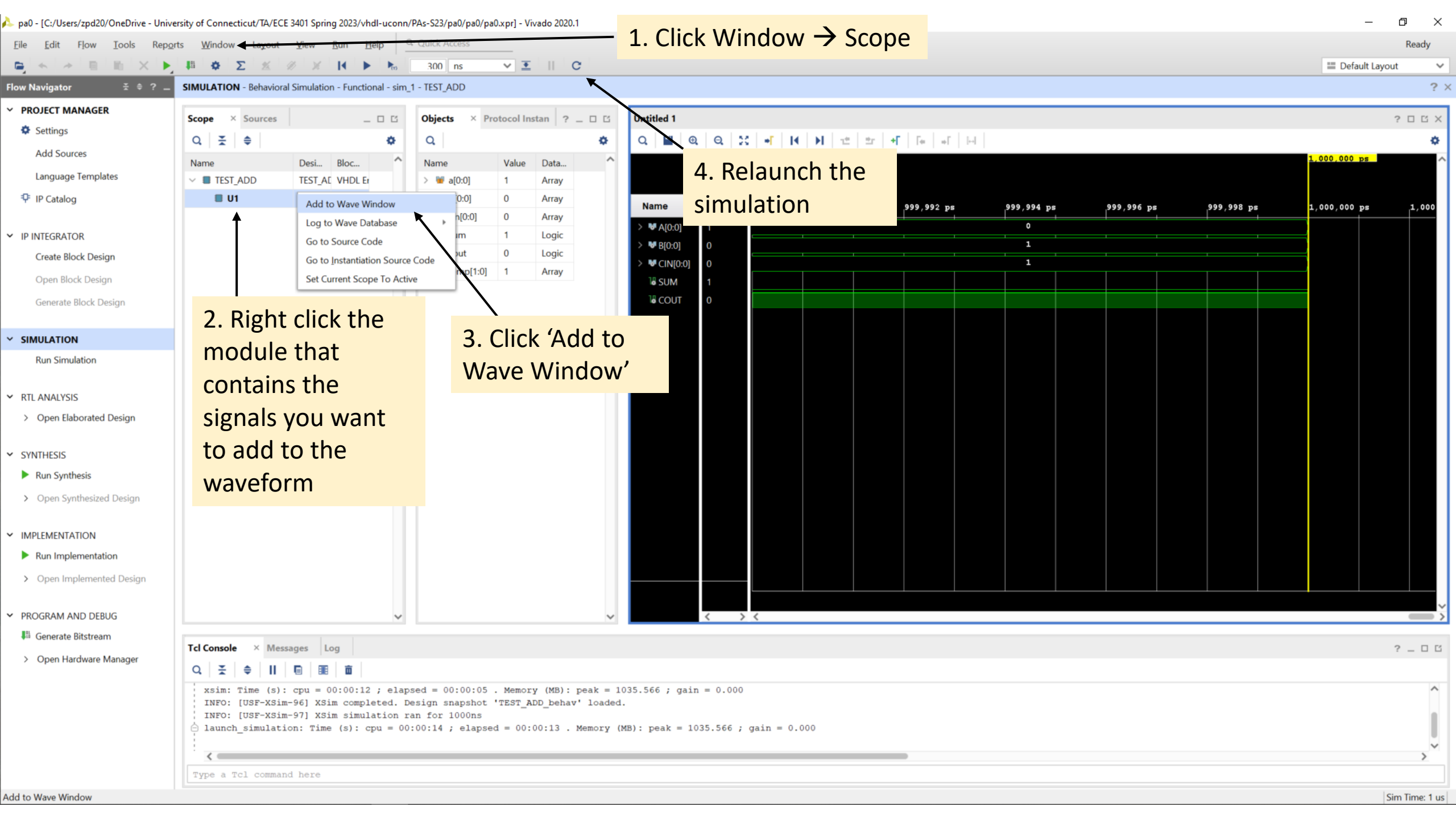
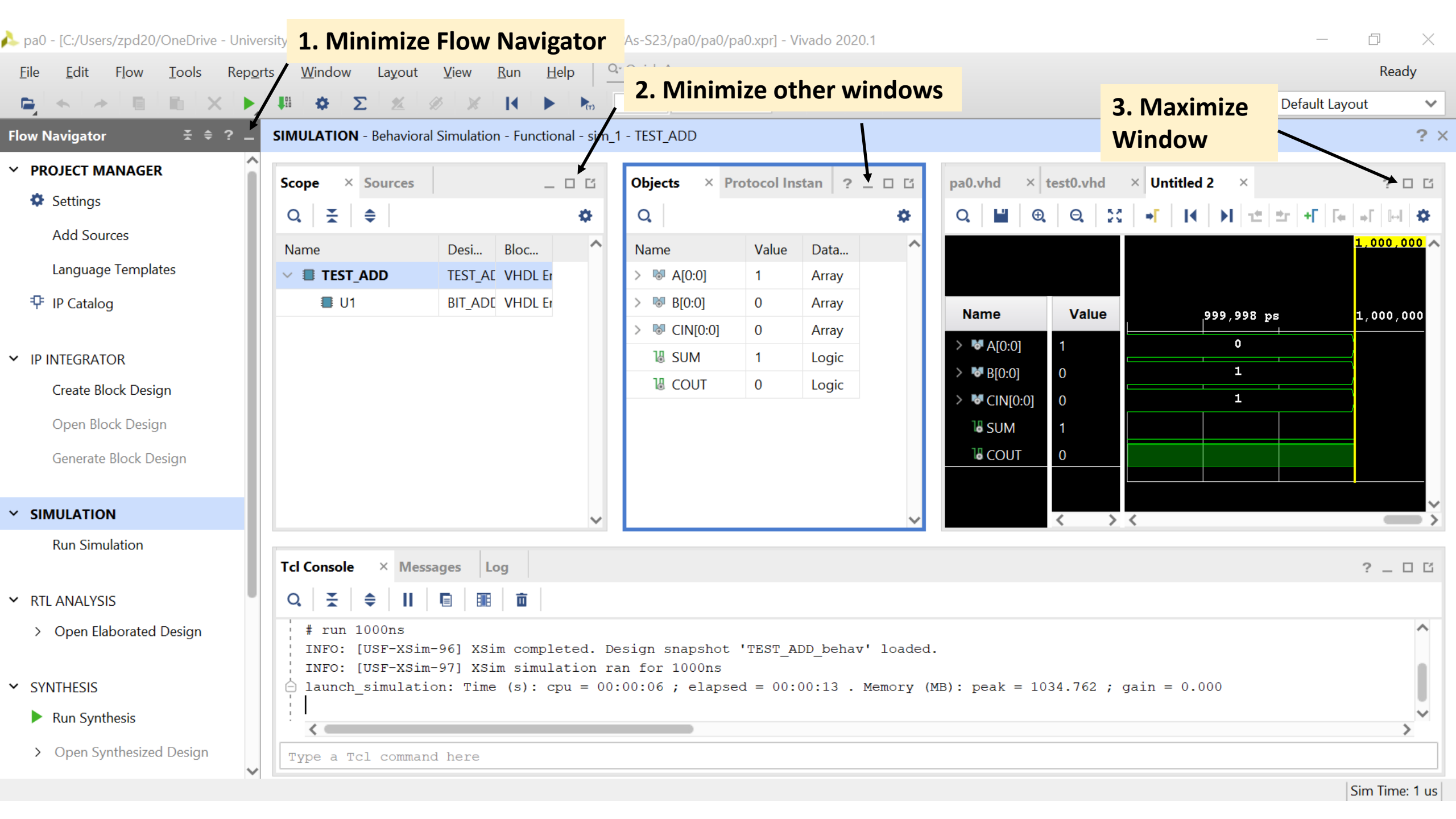
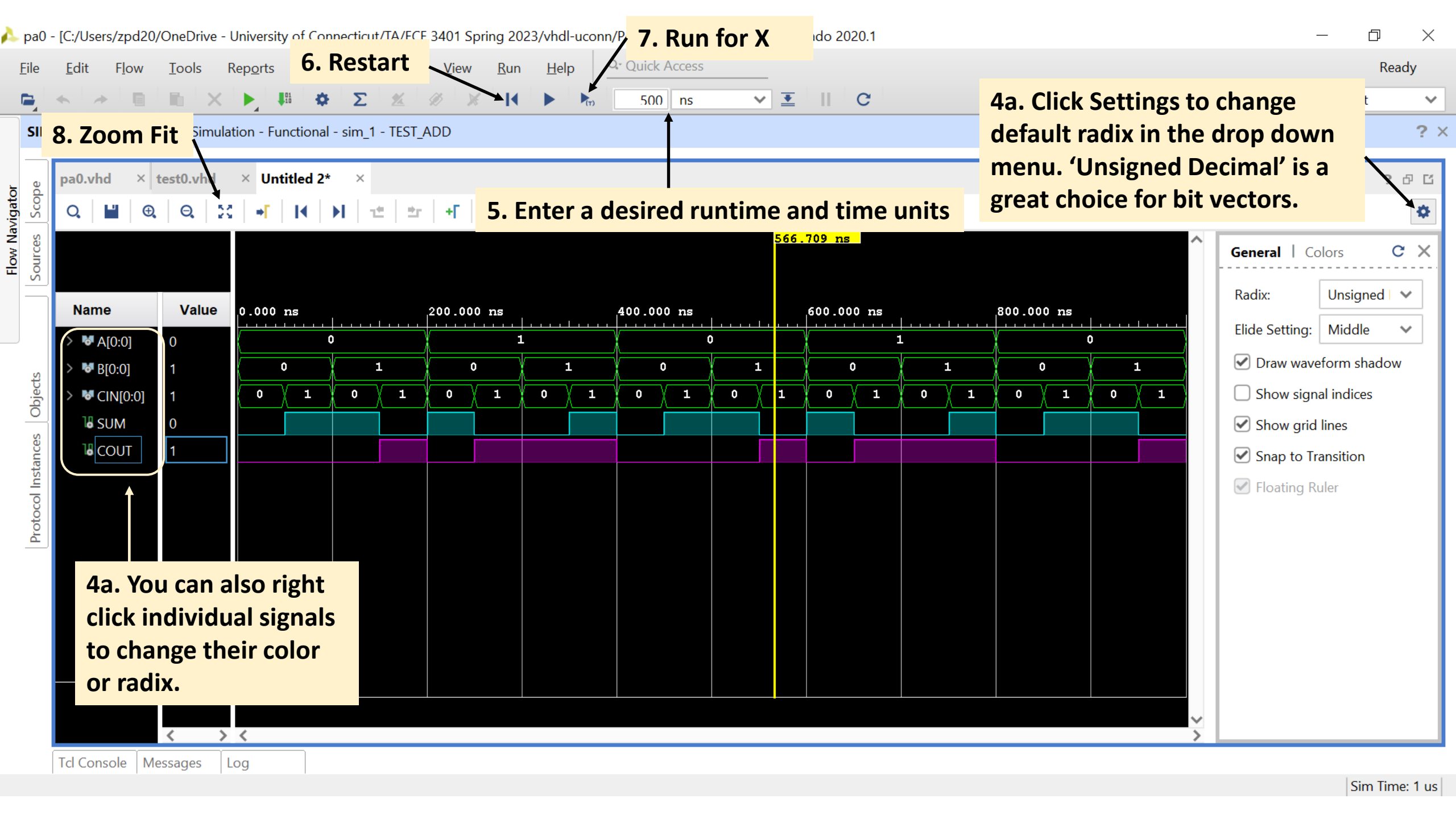
Part 1: Adding Signals to Your Waveform


pa0 - [C:/Users/zpd20/OneDrive - University of Connecticut/TA/ECE 3401 Spring 2023/vhdl-uconn/PAs-S23/pa0/pa0/pa0.xpr] - Vivado 2020.1
File Edit Flow Tools Reports Window Layout View Run Help
Ready
Default Layout
1. Click Window → Scope
Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager
SIMULATION - Behavioral Simulation - Functional - sim_1 - TEST_ADD
Scope
Sources
Objects
Protocol Instan
Name
Desi...
Bloc...
TEST_ADD
VHDL Er
U1
Add to Wave Window
Log to Wave Database
Go to Source Code
Go to Instantiation Source Code
Set Current Scope To Active
Value
Data...
a[0:0]
Array
Logic
2. Right click the module that contains the signals you want to add to the waveform
3. Click 'Add to Wave Window'
4. Relaunch the simulation
Untitled 1
1,000,000 ps
999,992 ps
999,994 ps
999,996 ps
999,998 ps
A[0:0]
B[0:0]
CIN[0:0]
SUM
COUT
Tcl Console
Messages
Log
xsim: Time (s): cpu = 00:00:12 ; elapsed = 00:00:05 . Memory (MB): peak = 1035.566 ; gain = 0.000
INFO: [USF-XSim-96] XSim completed. Design snapshot 'TEST_ADD_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
launch_simulation: Time (s): cpu = 00:00:14 ; elapsed = 00:00:13 . Memory (MB): peak = 1035.566 ; gain = 0.000
Type a Tcl command here
Add to Wave Window
Sim Time: 1 us

Part 2: Guidelines and Tips For Waveform Formatting


1. Minimize Flow Navigator
2. Minimize other windows
3. Maximize Window
pa0 - [C:/Users/zpd20/OneDrive - University
As-S23/pa0/pa0/pa0.xpr] - Vivado 2020.1
File
Edit
Flow
Tools
Reports
Window
Layout
View
Run
Help
Ready
Default Layout
Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
SIMULATION - Behavioral Simulation - Functional - sim_1 - TEST_ADD
Scope
Sources
Name
Desi...
Bloc...
TEST_ADD
TEST_AL
VHDL Er
U1
BIT_ADL
VHDL Er
Objects
Protocol Instan
Name
Value
Data...
A[0:0]
1
Array
B[0:0]
0
Array
CIN[0:0]
0
Array
SUM
1
Logic
COUT
0
Logic
pa0.vhd
test0.vhd
Untitled 2
Name
Value
A[0:0]
1
B[0:0]
0
CIN[0:0]
0
SUM
1
COUT
0
999,998 ps
1,000,000
1,000,000
0
1
1
Tcl Console
Messages
Log
run 1000ns
INFO: [USF-XSim-96] XSim completed. Design snapshot 'TEST_ADD_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
launch_simulation: Time (s): cpu = 00:00:06 ; elapsed = 00:00:13 . Memory (MB): peak = 1034.762 ; gain = 0.000
Type a Tcl command here
Sim Time: 1 us


7. Run for X
6. Restart
8. Zoom Fit
5. Enter a desired runtime and time units
4a. Click Settings to change default radix in the drop down menu. 'Unsigned Decimal' is a great choice for bit vectors.
4a. You can also right click individual signals to change their color or radix.
pa0 - [C:/Users/zpd20/OneDrive - University of Connecticut/TA/ECE 3401 Spring 2023/vhdl-uconn/P
do 2020.1
File
Edit
Flow
Tools
Reports
View
Run
Help
Quick Access
Ready
500
ns
Simulation - Functional - sim_1 - TEST_ADD
pa0.vhd
test0.vhd
Untitled 2*
Flow Navigator
Scope
Sources
Objects
Protocol Instances
Name
Value
A[0:0]
B[0:0]
CIN[0:0]
SUM
COUT
0
1
1
0
1
566.709 ns
0.000 ns
200.000 ns
400.000 ns
600.000 ns
800.000 ns
General
Colors
Radix:
Unsigned
Elide Setting:
Middle
Draw waveform shadow
Show signal indices
Show grid lines
Snap to Transition
Floating Ruler
Tcl Console
Messages
Log
Sim Time: 1 us