PA0 Guide

ECE 3401/CSE 3302 – Spring 2024

Course TA contact information:

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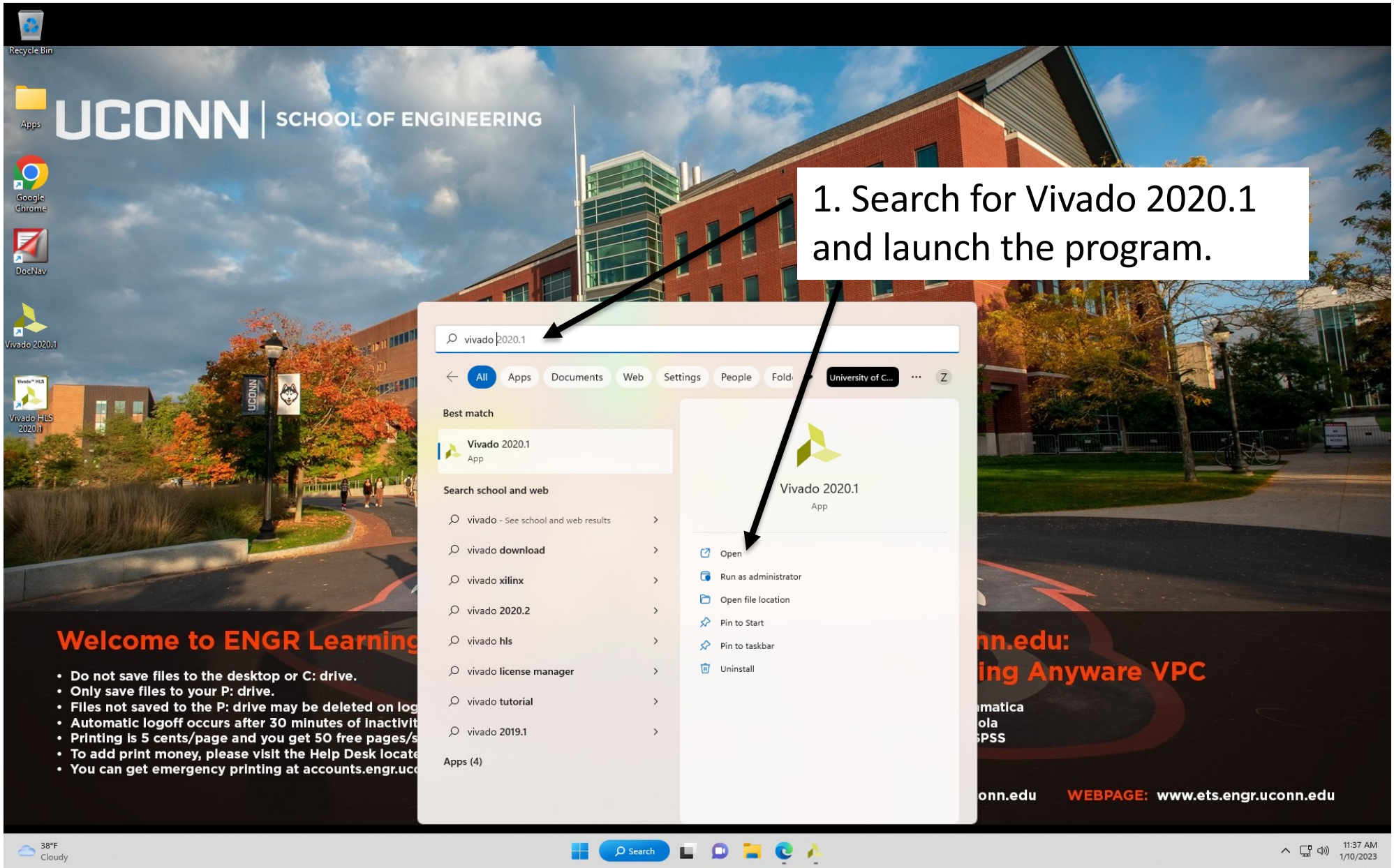
Getting Started

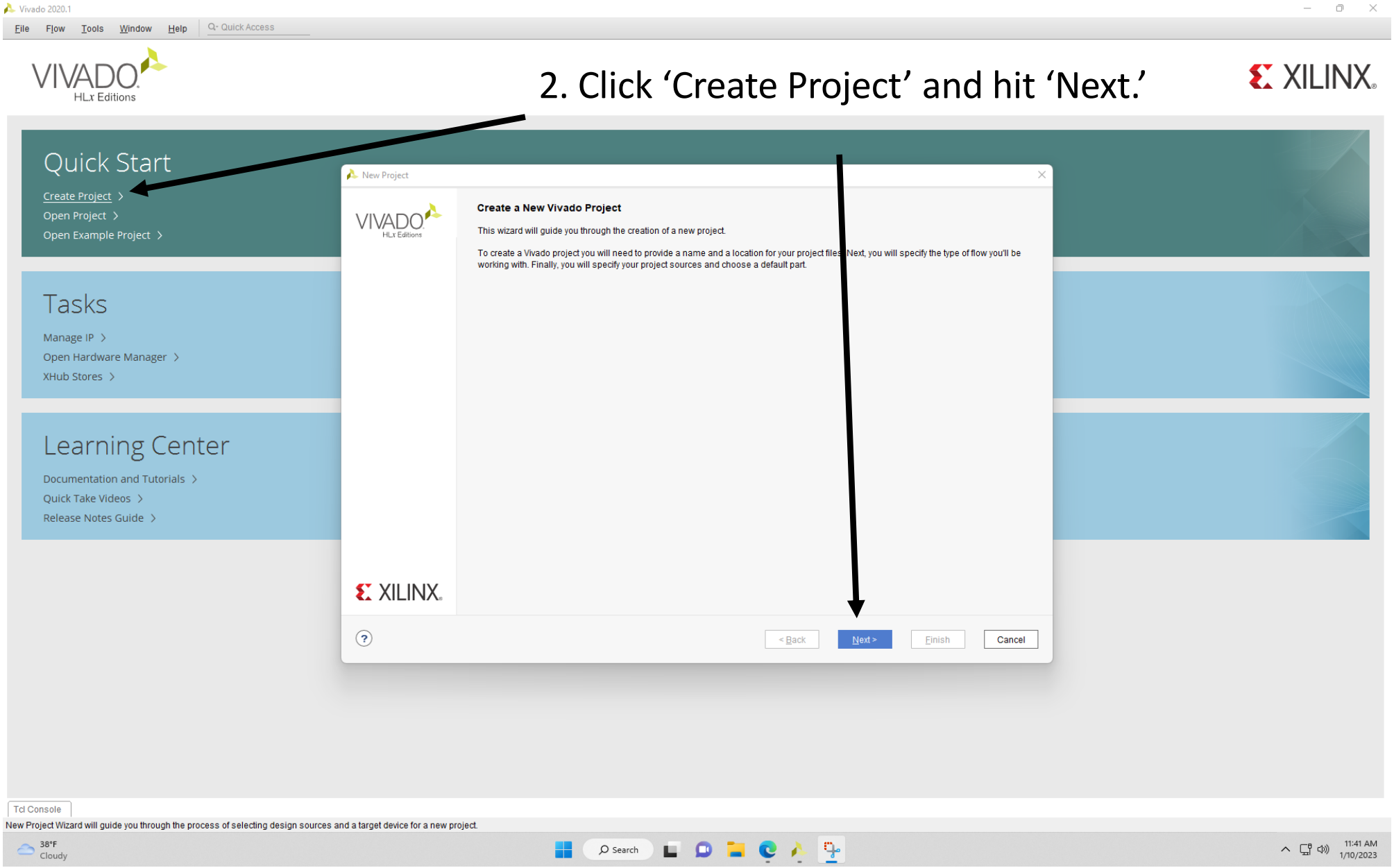
At this point, it is assumed you either

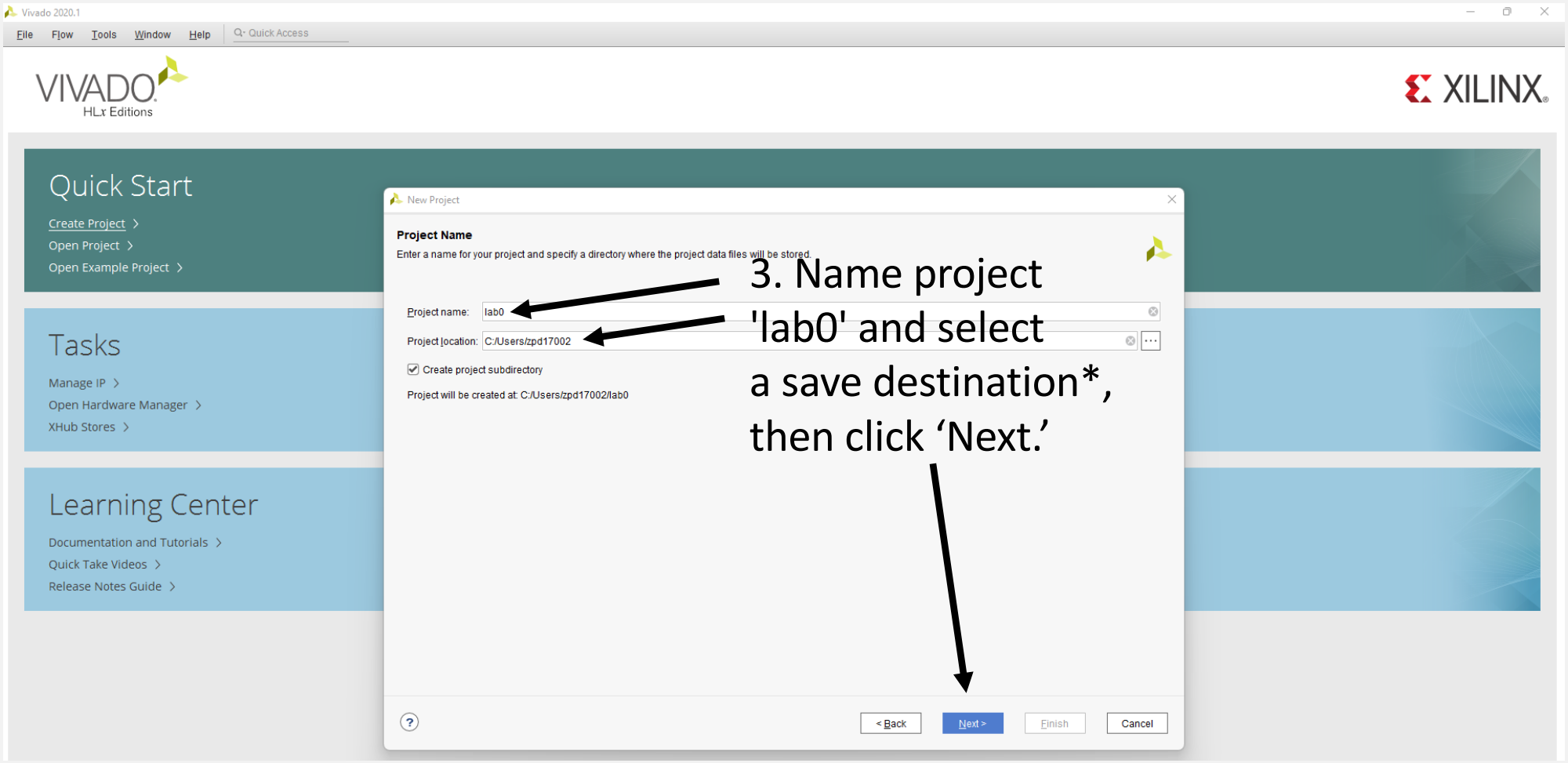
1. Have Vivado downloaded on your personal computer
2. Are connected to an SoE computer via UConn Anyware
3. Are in E2 305/306/307 and are using one of the provided desktops

If you haven't already, go through the Vivado toolchain guide to get started with the software we will use.


1. Search for Vivado 2020.1 and launch the program.
vivado 2020.1
All
Apps
Documents
Web
Settings
People
Best match
Vivado 2020.1
App
Search school and web
vivado - See school and web results
vivado download
vivado xilinx
vivado 2020.2
vivado hls
vivado license manager
vivado tutorial
vivado 2019.1
Apps (4)
Vivado 2020.1
App
Open
Run as administrator
Open file location
Pin to Start
Pin to taskbar
Uninstall
Welcome to ENGR Learning
Do not save files to the desktop or C: drive.
Only save files to your P: drive.
Files not saved to the P: drive may be deleted on log
Automatic logoff occurs after 30 minutes of inactivit
Printing is 5 cents/page and you get 50 free pages/s
To add print money, please visit the Help Desk locate
You can get emergency printing at accounts.engr.uc
nn.edu:
ing Anyware VPC
matica
ola
SPSS
onn.edu
WEBPAGE: www.ets.engr.uconn.edu
38°F
Cloudy
Search
11:37 AM
1/10/2023

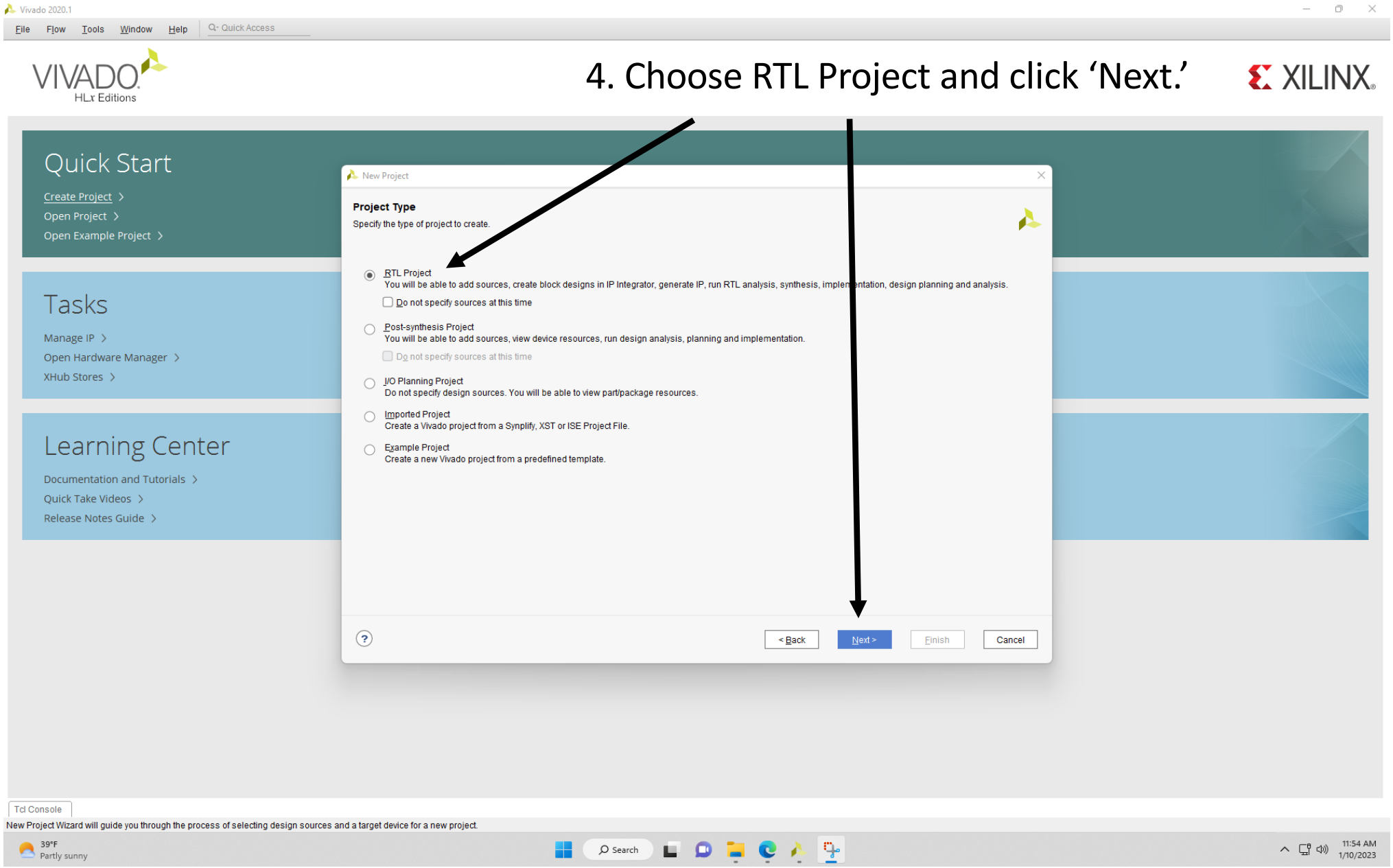
2. Click ‘Create Project’ and hit ‘Next.’

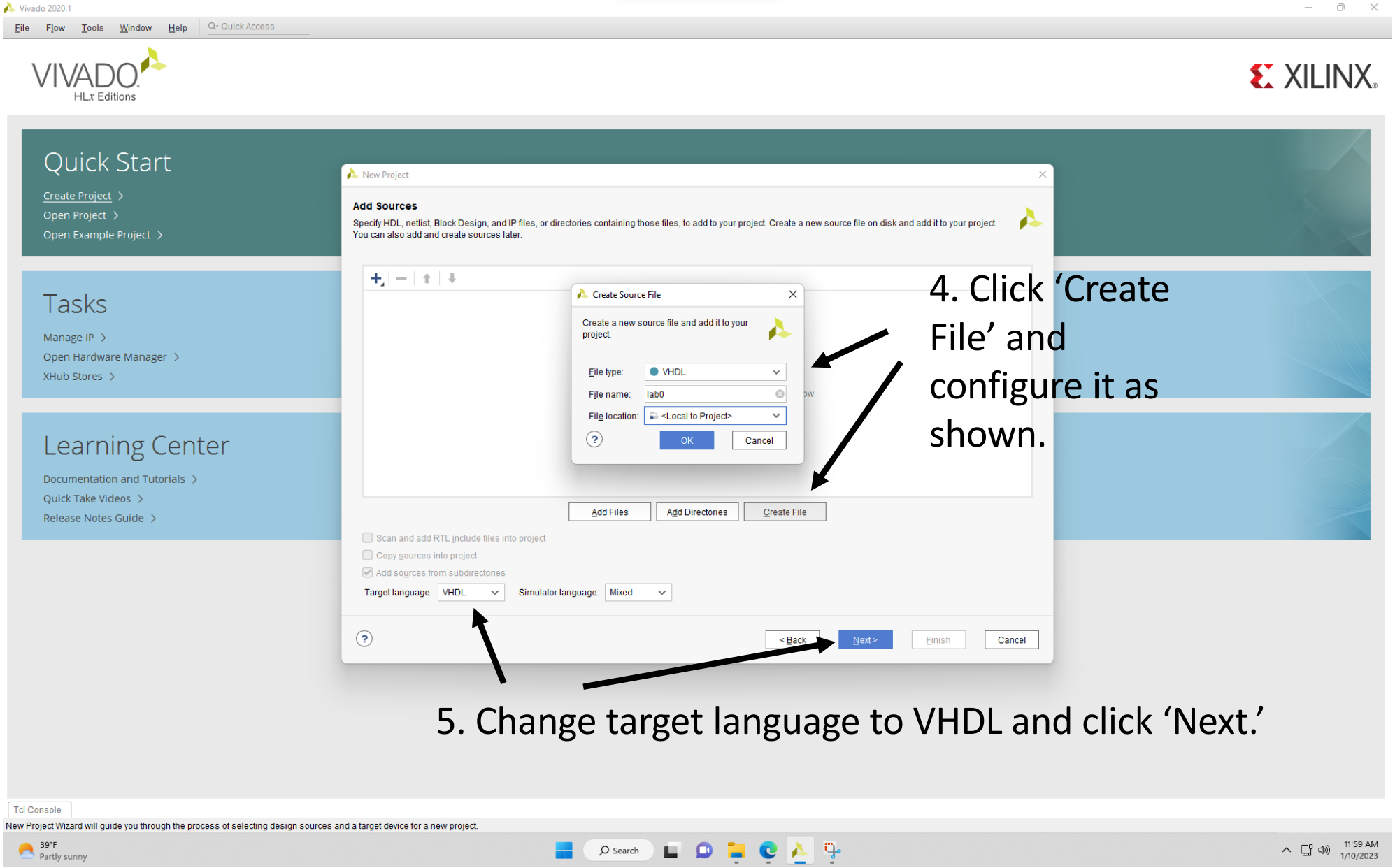


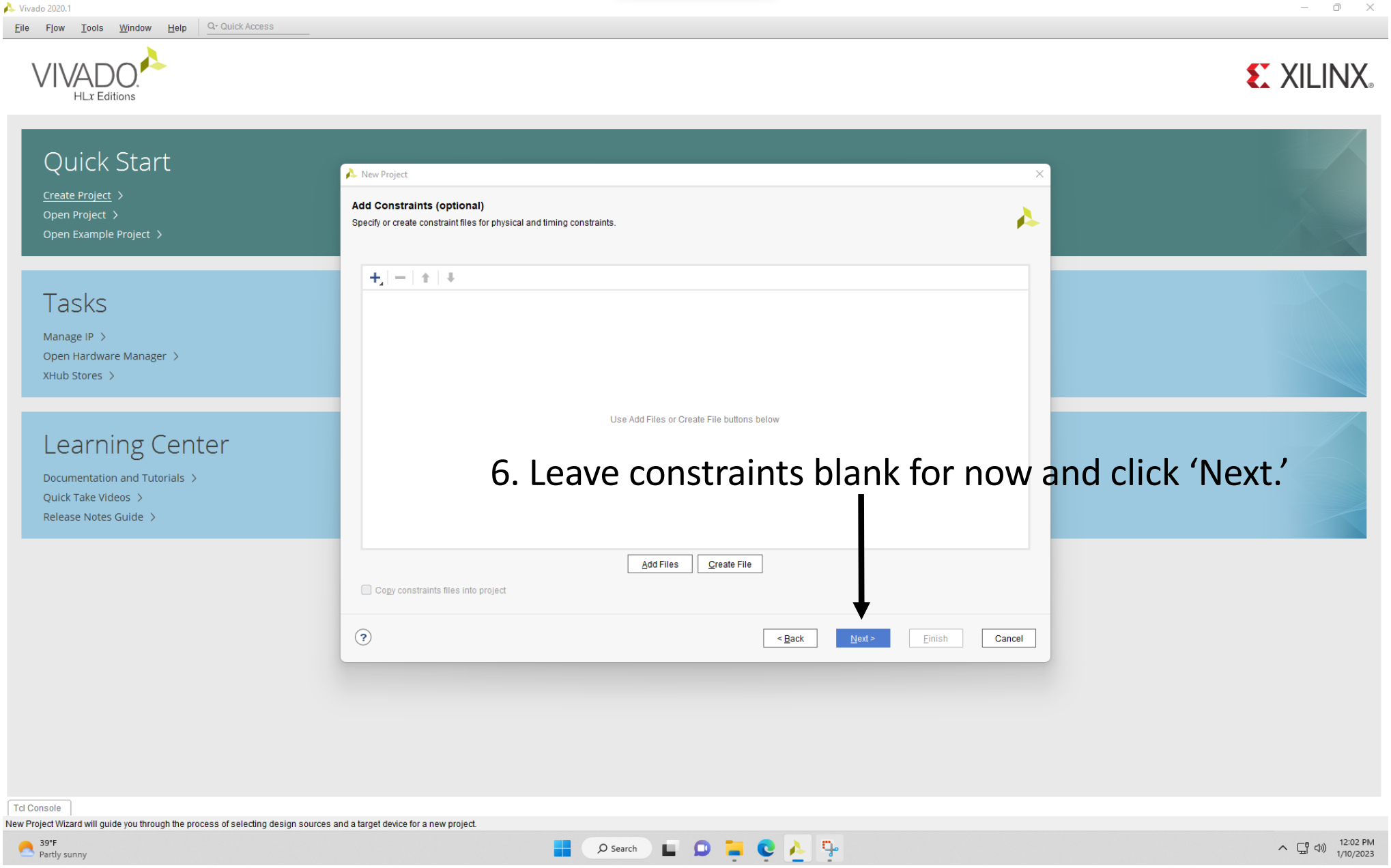


*As of Jan 10, 2023, the P: drive is discontinued. When working on UConn Anyware / E2 computers, files saved at 'C:/Users/abc12345/...' **will remain saved** after logging off. If you plan on working on both personal and UConn computers, you should also consider saving to OneDrive. Saving to OneDrive will allow you to access files through a synced folder accessible through your personal computer and UConn Anyware desktop.

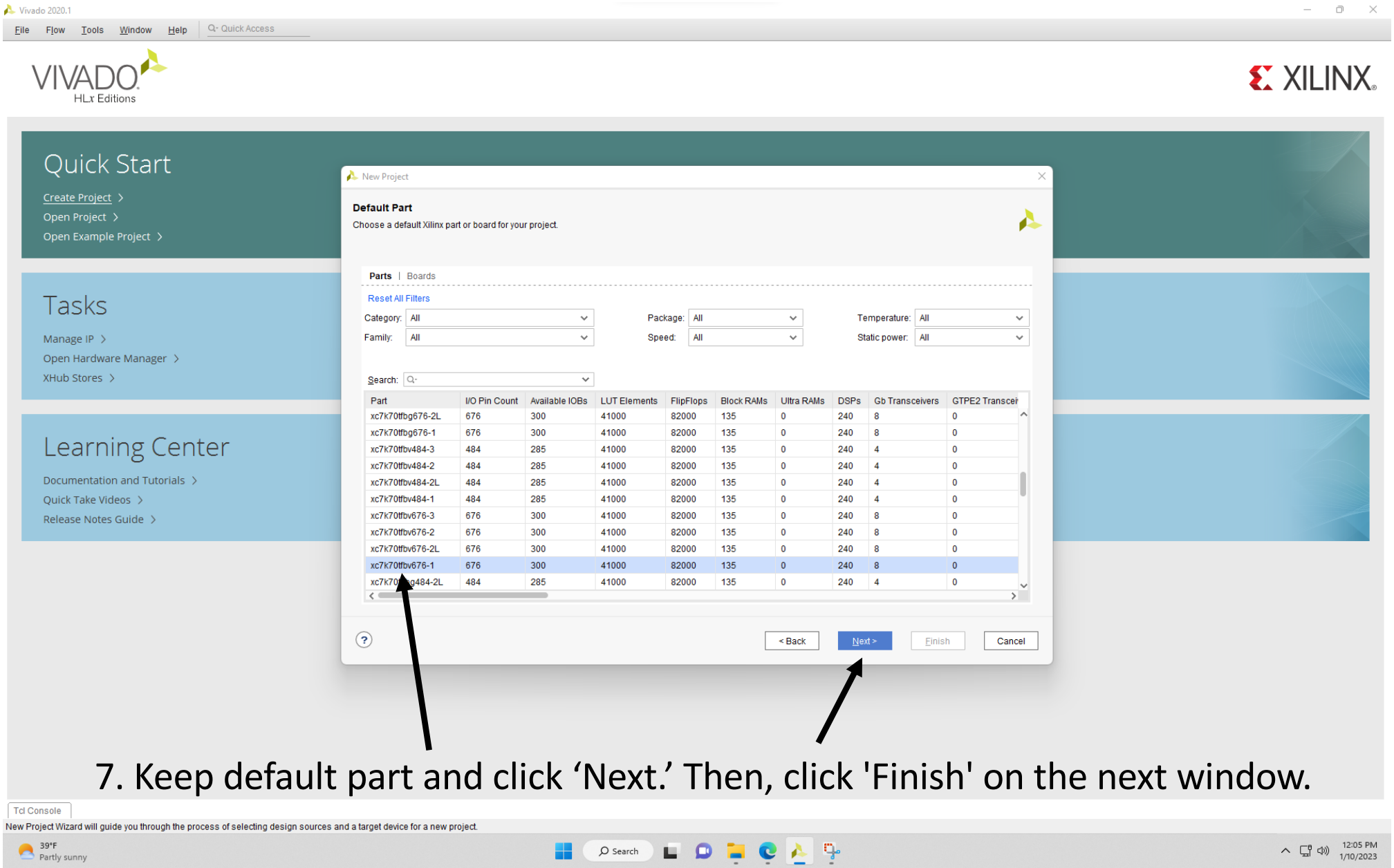
4. Choose RTL Project and click ‘Next.’



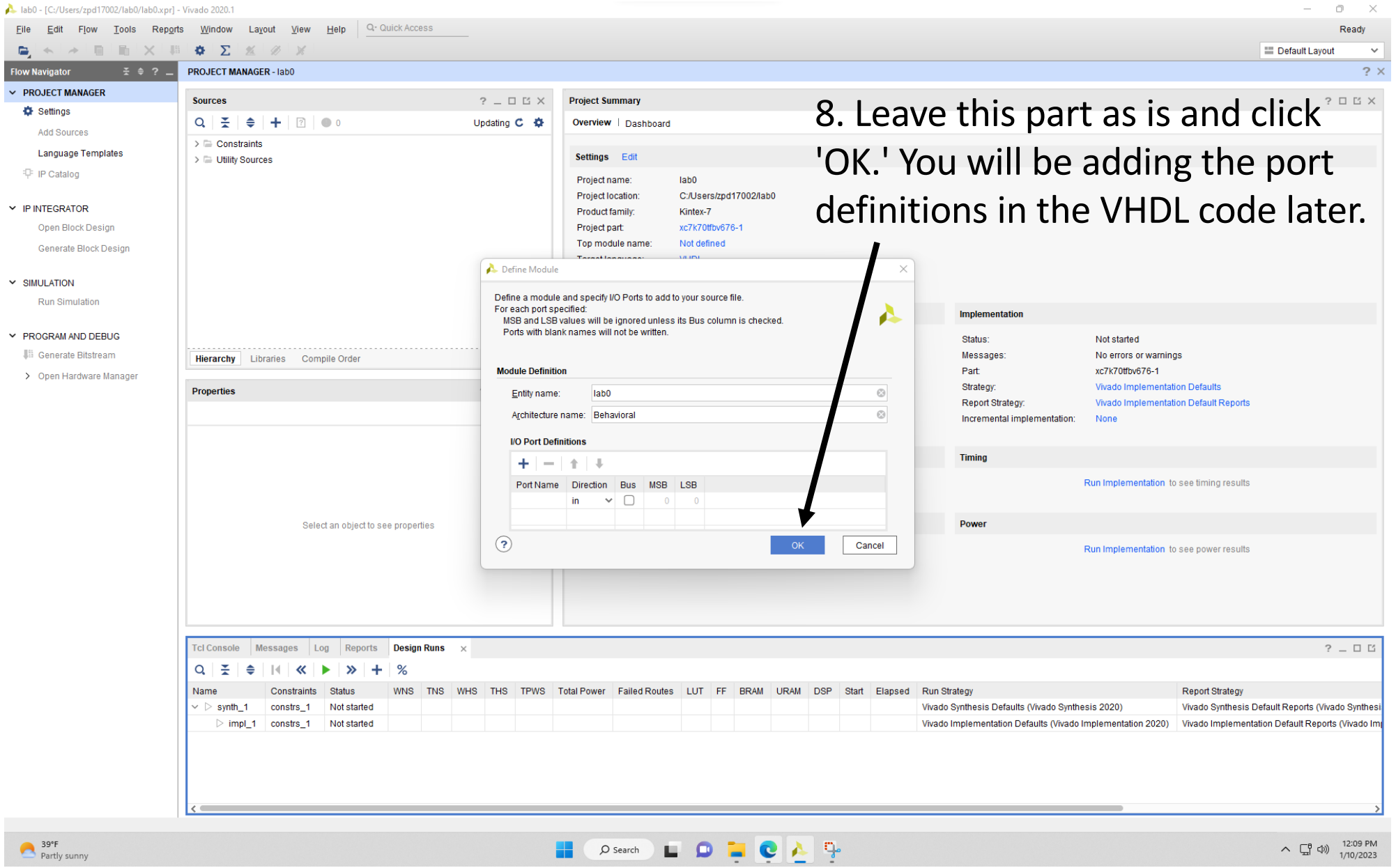

Vivado 2020.1
File Flow Tools Window Help Quick Access
VIVADO HLx Editions
XILINX
Quick Start
Create Project
Open Project
Open Example Project
Tasks
Manage IP
Open Hardware Manager
XHub Stores
Learning Center
Documentation and Tutorials
Quick Take Videos
Release Notes Guide
New Project
Add Sources
Specify HDL, netlist, Block Design, and IP files, or directories containing those files, to add to your project. Create a new source file on disk and add it to your project.
You can also add and create sources later.
Create Source File
Create a new source file and add it to your project.
File type: VHDL
File name: lab0
File location: <Local to Project>
OK
Cancel
Add Files
Add Directories
Create File
Scan and add RTL include files into project
Copy sources into project
Add sources from subdirectories
Target language: VHDL
Simulator language: Mixed
< Back
Next >
Finish
Cancel
4. Click 'Create File' and configure it as shown.
5. Change target language to VHDL and click 'Next.'
Tcl Console
New Project Wizard will guide you through the process of selecting design sources and a target device for a new project.
39°F Partly sunny
Search
11:59 AM 1/10/2023



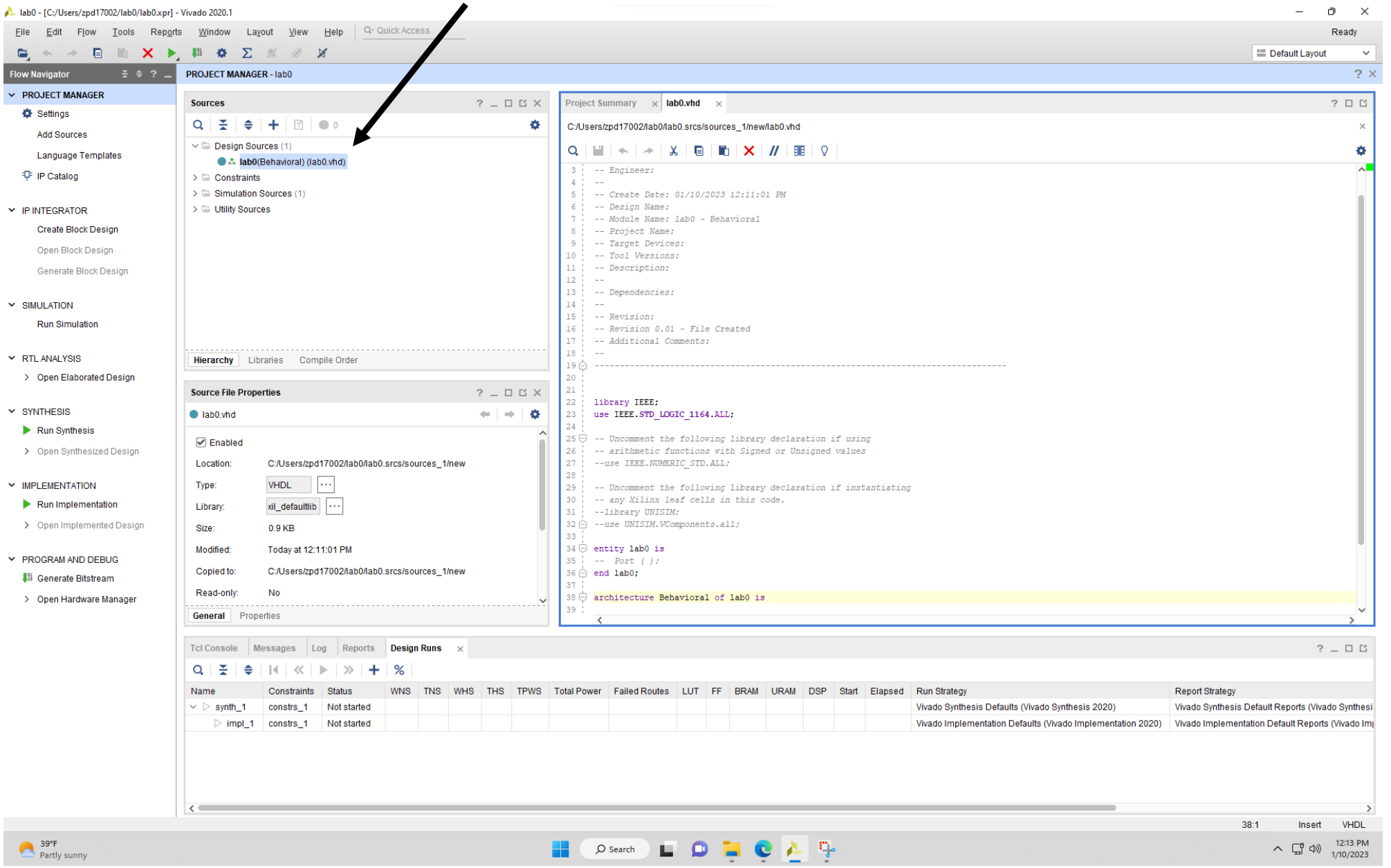
6. Leave constraints blank for now and click ‘Next.’

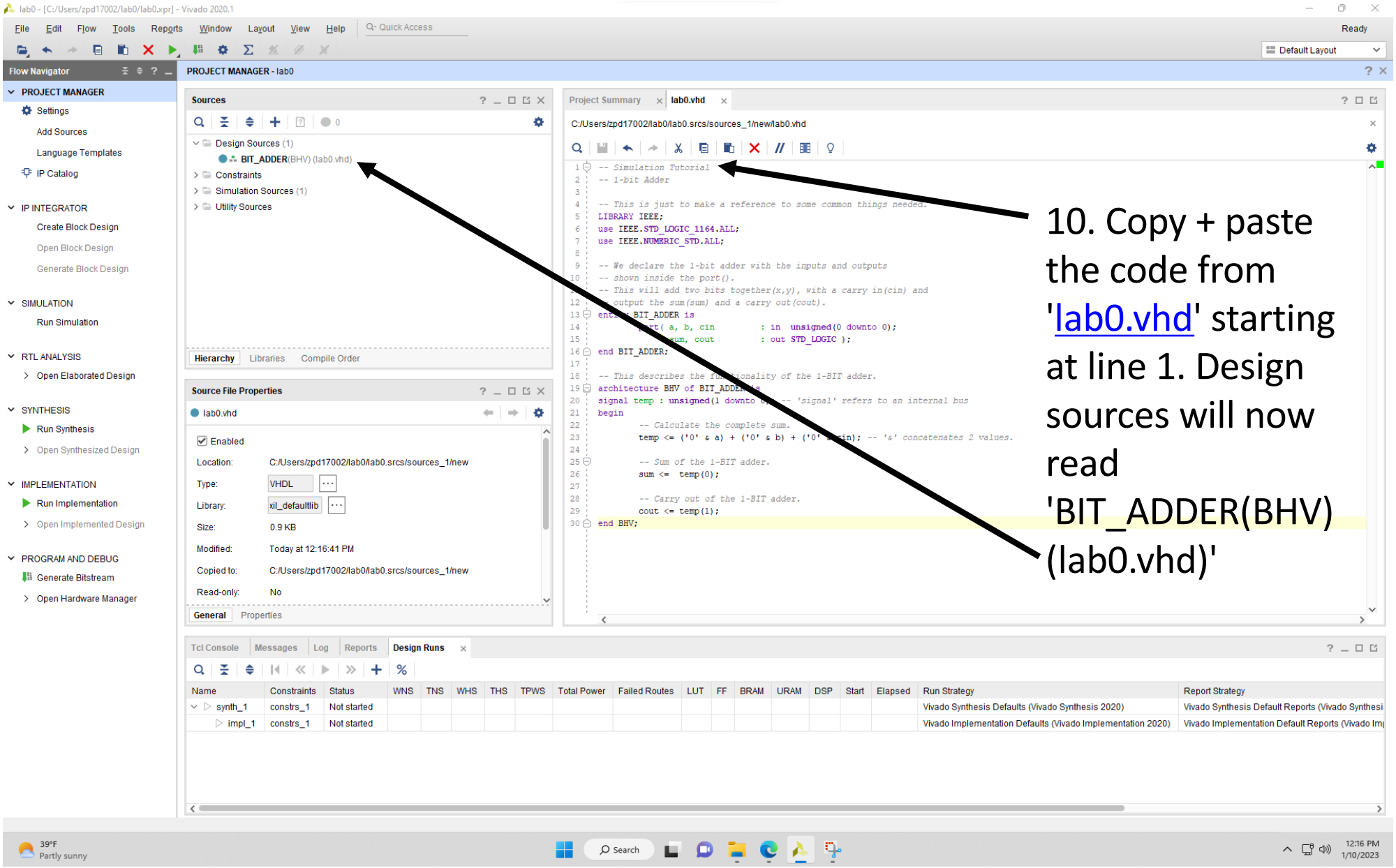


7. Keep default part and click ‘Next.’ Then, click 'Finish' on the next window.


8. Leave this part as is and click 'OK.' You will be adding the port definitions in the VHDL code later.
Define Module
Define a module and specify I/O Ports to add to your source file.
For each port specified:
MSB and LSB values will be ignored unless its Bus column is checked.
Ports with blank names will not be written.
Module Definition
Entity name: lab0
Architecture name: Behavioral
I/O Port Definitions
Port Name
Direction
Bus
MSB
LSB
OK
Cancel

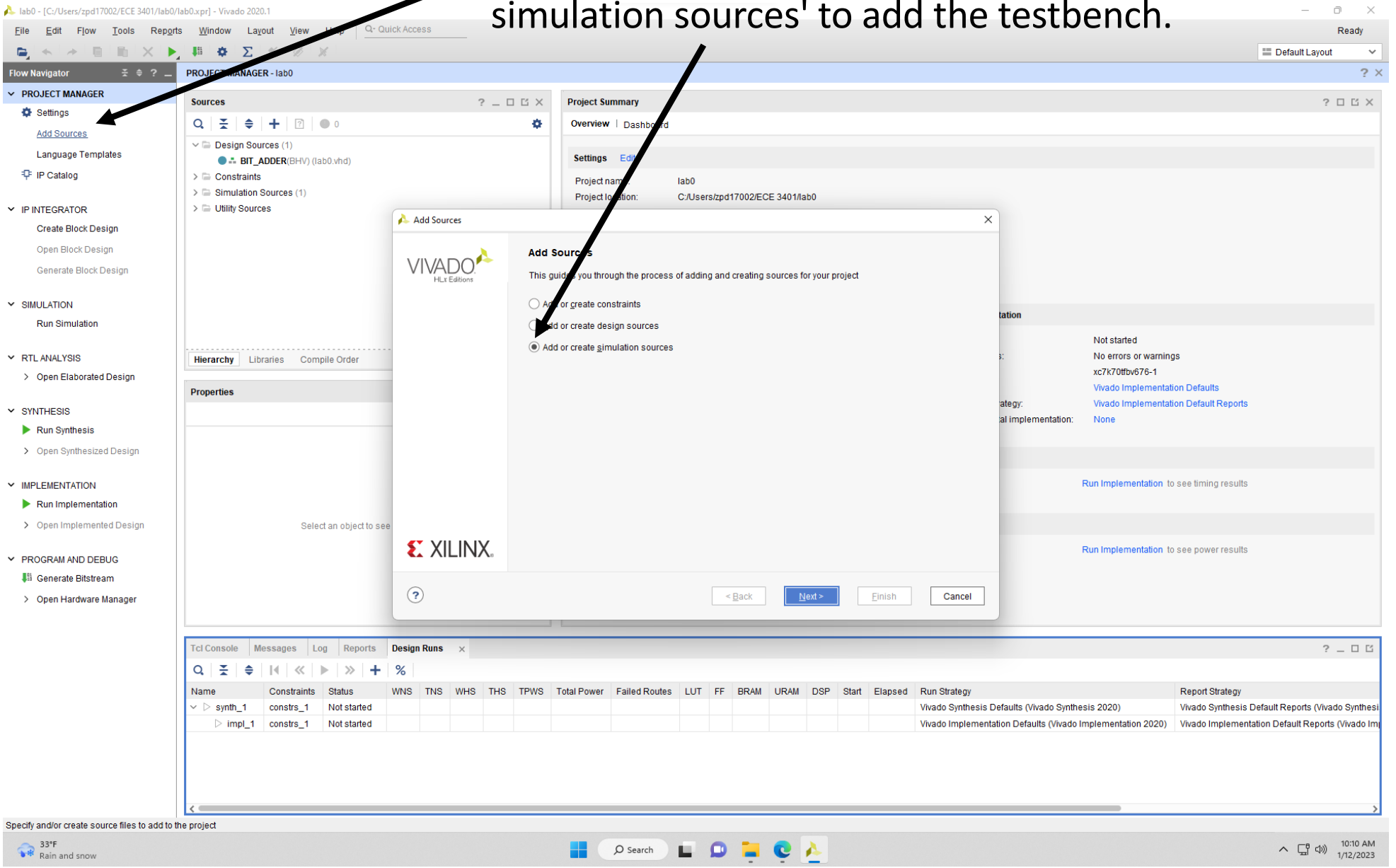
9. Double click 'lab0(Behavioral) (lab0.vhd)' to open the project file.

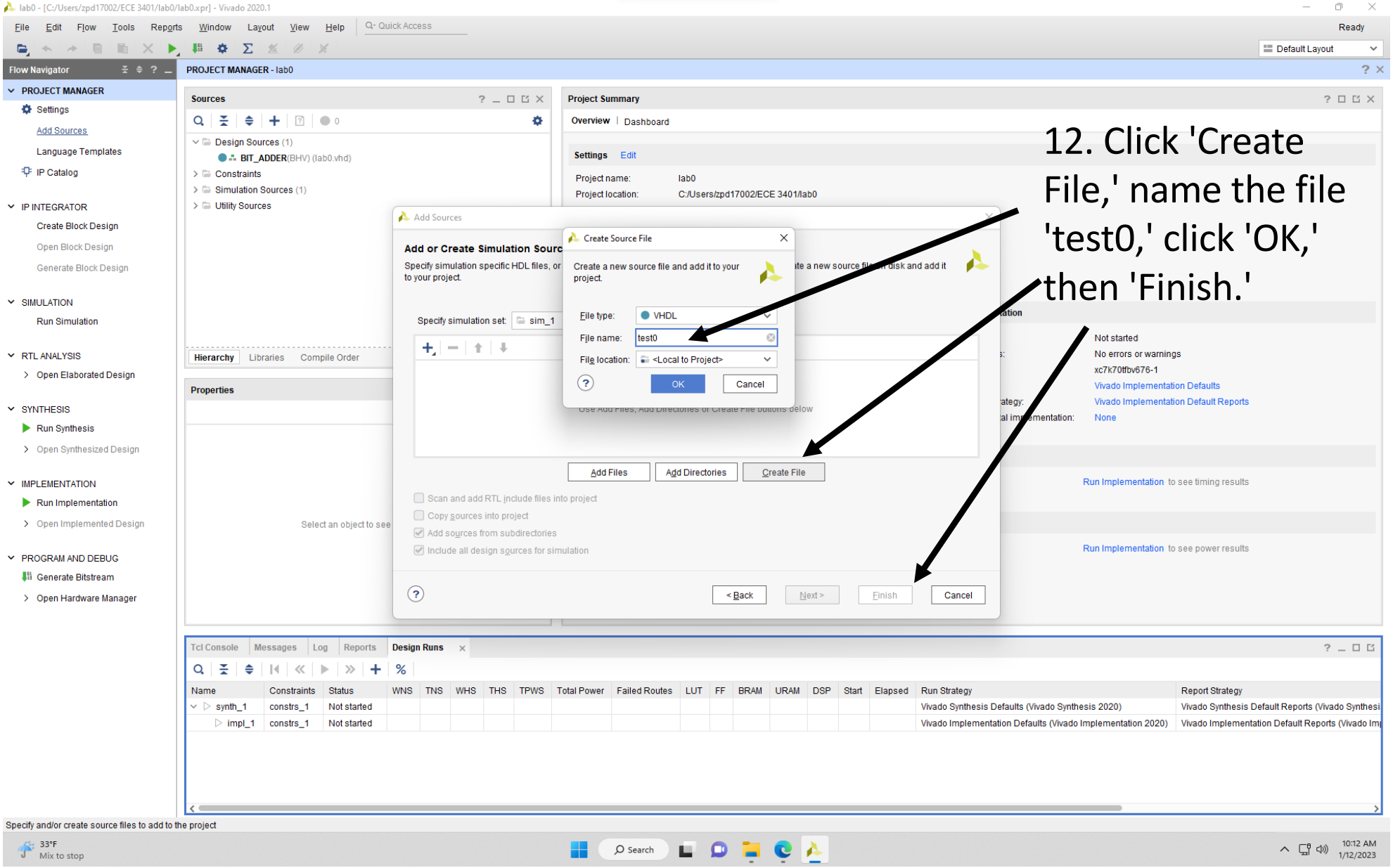


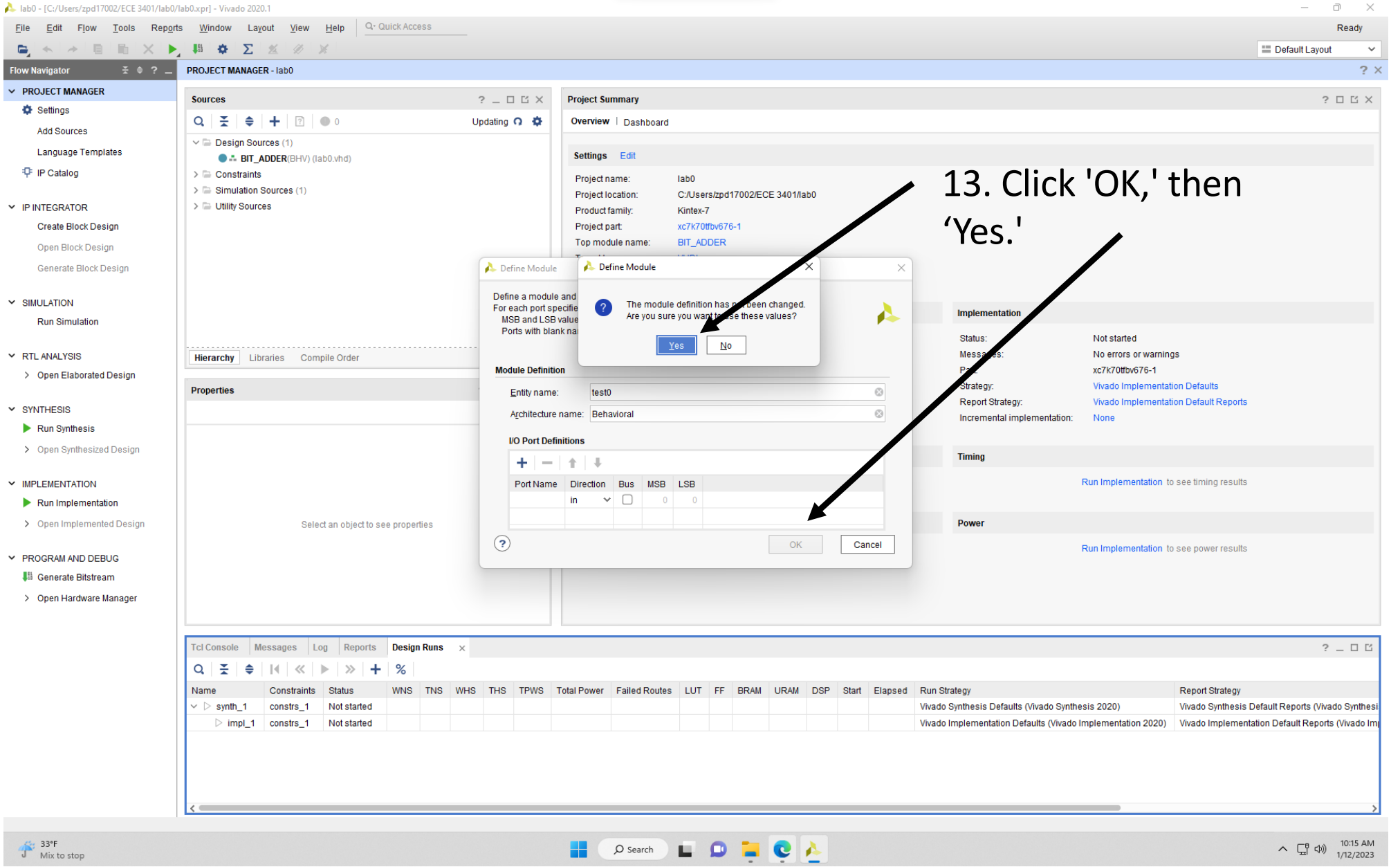


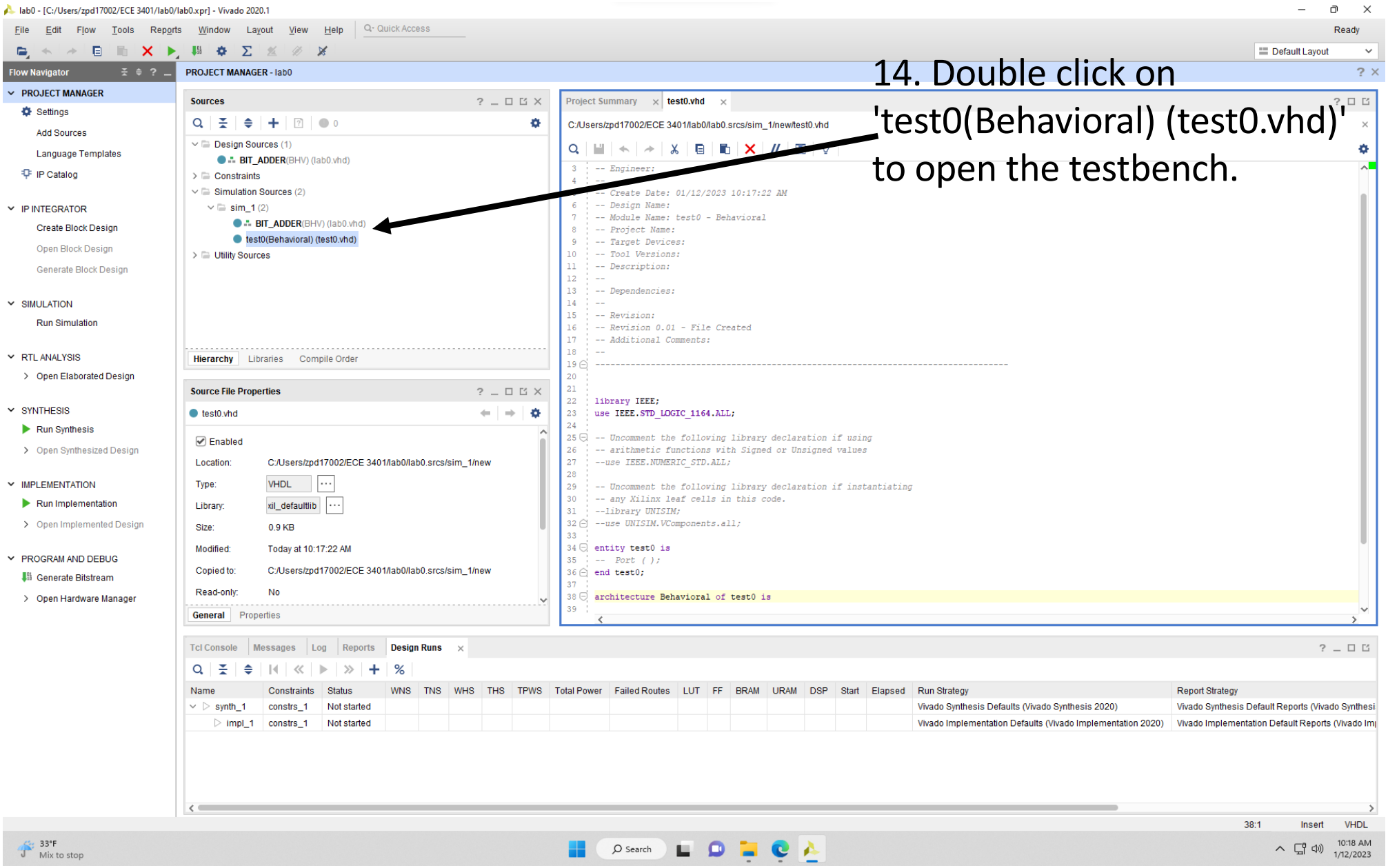
10. Copy + paste the code from '[lab0.vhd](lab0.vhd)' starting at line 1. Design sources will now read 'BIT_ADDER(BHV) (lab0.vhd)'

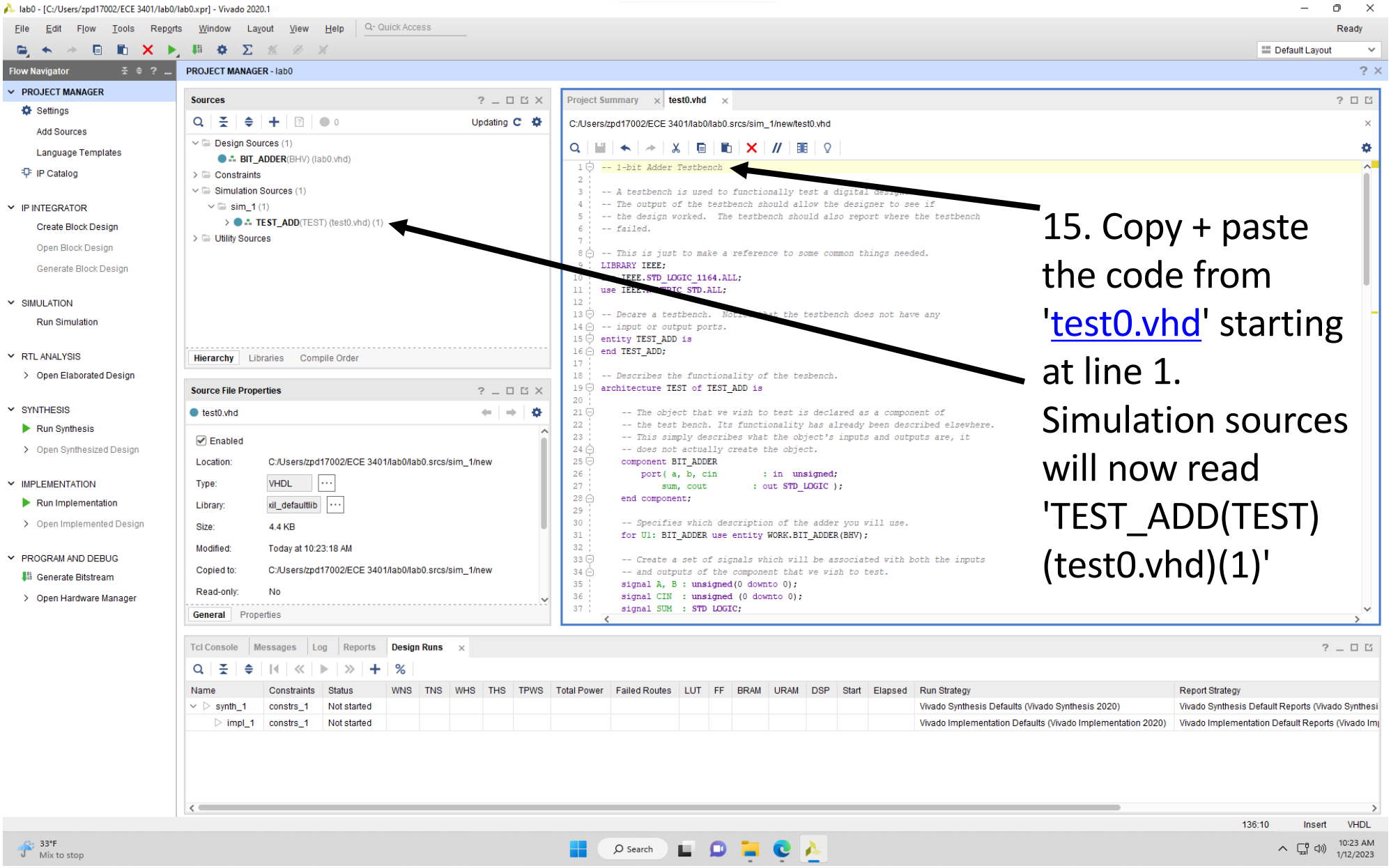
11. Click 'Add Sources' then 'Add or create simulation sources' to add the testbench.




12. Click 'Create File,' name the file 'test0,' click 'OK,' then 'Finish.'


13. Click 'OK,' then 'Yes.'
Define Module
The module definition has not been changed.
Are you sure you want to use these values?
Yes
No
Module Definition
Entity name: test0
Architecture name: Behavioral
I/O Port Definitions
Port Name
Direction
Bus
MSB
LSB
OK
Cancel


14. Double click on 'test0(Behavioral) (test0.vhd)' to open the testbench.
lab0 - [C:/Users/zpd17002/ECE 3401/lab0/lab0.xpr] - Vivado 2020.1
File Edit Flow Tools Reports Window Layout View Help
Quick Access
Ready
Default Layout
Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager
PROJECT MANAGER - lab0
Sources
Design Sources (1)
BIT_ADDER(BHV) (lab0.vhd)
Constraints
Simulation Sources (2)
sim_1 (2)
BIT_ADDER(BHV) (lab0.vhd)
test0(Behavioral) (test0.vhd)
Utility Sources
Hierarchy Libraries Compile Order
Source File Properties
test0.vhd
Enabled
Location: C:/Users/zpd17002/ECE 3401/lab0/lab0.srcs/sim_1/new
Type: VHDL
Library: xil_defaultlib
Size: 0.9 KB
Modified: Today at 10:17:22 AM
Copied to: C:/Users/zpd17002/ECE 3401/lab0/lab0.srcs/sim_1/new
Read-only: No
General Properties
Project Summary
test0.vhd
C:/Users/zpd17002/ECE 3401/lab0/lab0.srcs/sim_1/new/test0.vhd
-- Engineer:
-- Create Date: 01/12/2023 10:17:22 AM
-- Design Name:
-- Module Name: test0 - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
-- Dependencies:
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;
-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;
entity test0 is
-- Port ( );
end test0;
architecture Behavioral of test0 is
Tcl Console Messages Log Reports Design Runs
Name Constraints Status WNS TNS WHS THS TPWS Total Power Failed Routes LUT FF BRAM URAM DSP Start Elapsed Run Strategy Report Strategy
synth_1 constrs_1 Not started Vivado Synthesis Defaults (Vivado Synthesis 2020) Vivado Synthesis Default Reports (Vivado Synthesi
impl_1 constrs_1 Not started Vivado Implementation Defaults (Vivado Implementation 2020) Vivado Implementation Default Reports (Vivado Im
38:1 Insert VHDL
33°F Mix to stop
Search
10:18 AM 1/12/2023



15. Copy + paste the code from 'test0.vhd' starting at line 1. Simulation sources will now read 'TEST_ADD(TEST)(test0.vhd)(1)'

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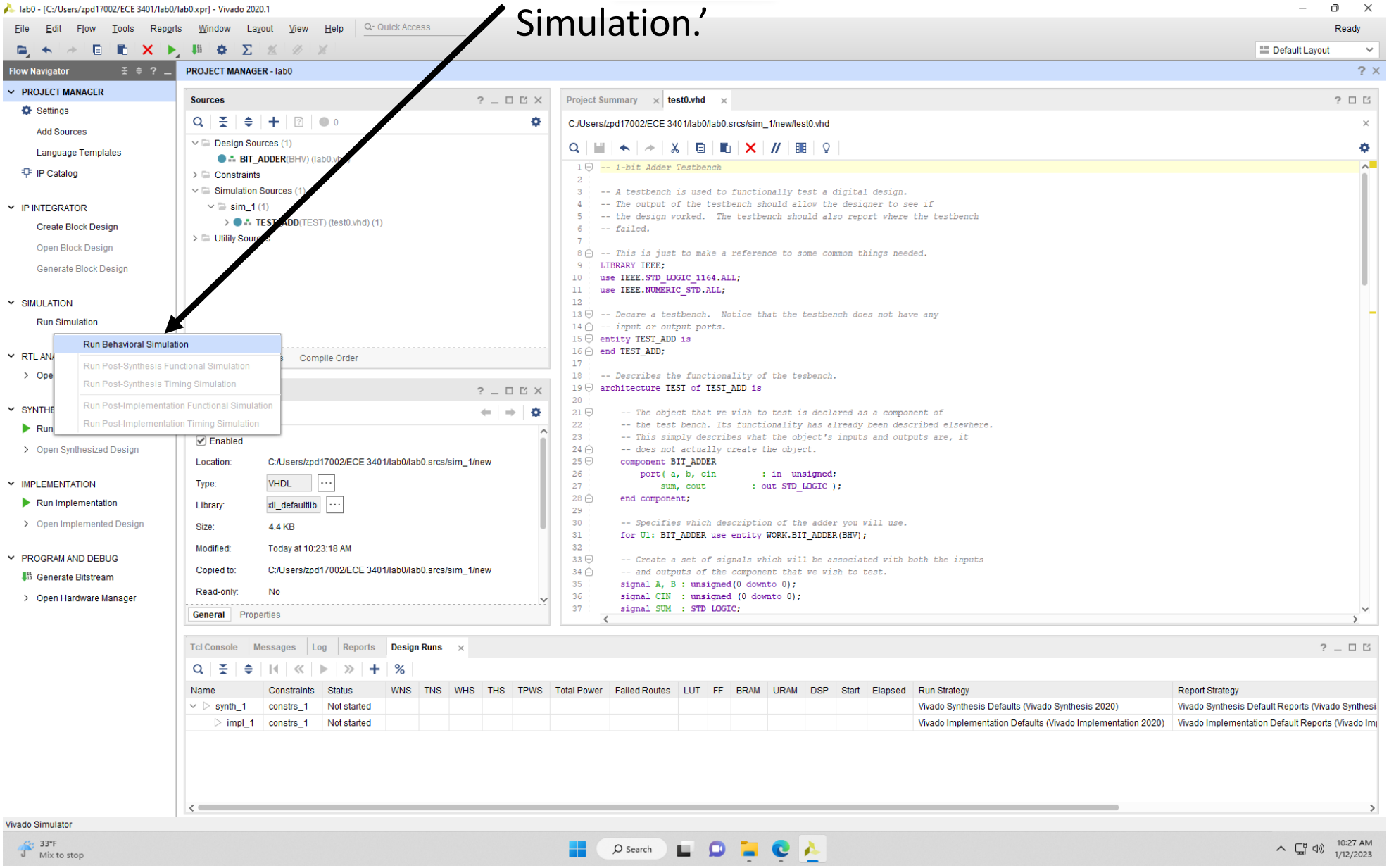
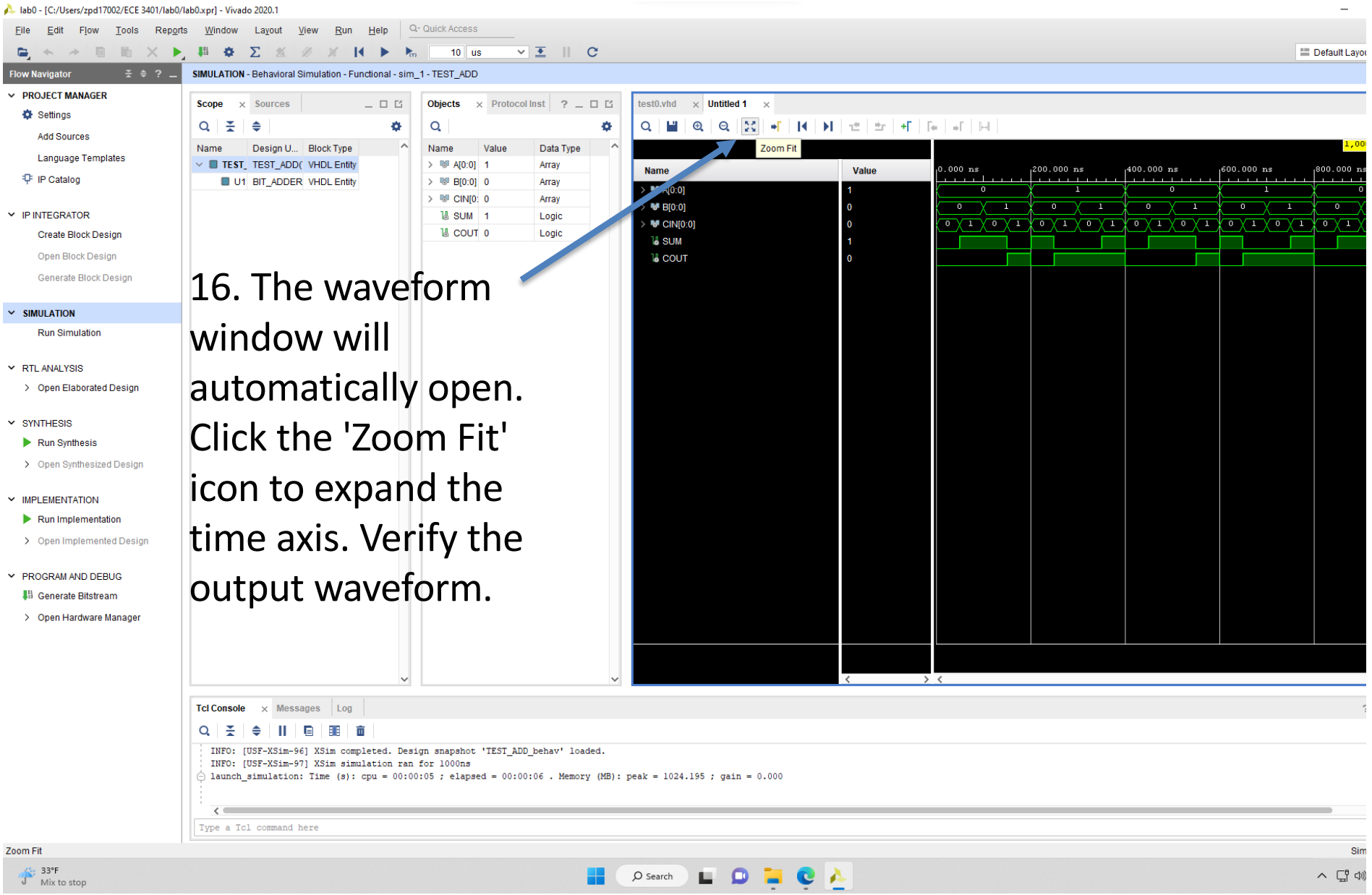
16. Click 'Run Simulation' then 'Run Behavioral Simulation.'





16. The waveform window will automatically open. Click the 'Zoom Fit' icon to expand the time axis. Verify the output waveform.

Questions

1. In BIT_ADDER(BHV) (lab0.vhd) what ...
   a. is the purpose of the 'entity' declaration (line 13)?
   b. is the purpose the 'architecture' declaration (line 19)?

2. In TEST_ADD(TEST) (test0.vhd)(1)…
   a. what is the purpose of the 'component' declaration (line 25)?
   b. what line # imports the functionality of the bit adder?
   c. once the bit adder becomes instantiated, what line # maps the declared signals to the input/output ports of the adder?

Deliverables

Please submit a single PDF of the following:

1. A screenshot of the window shown in the slide 19
2. Your answers to the questions in slide 20