

PA0 Guide

ECE 3401/CSE 3302 – Spring 2024

Course TA contact information:

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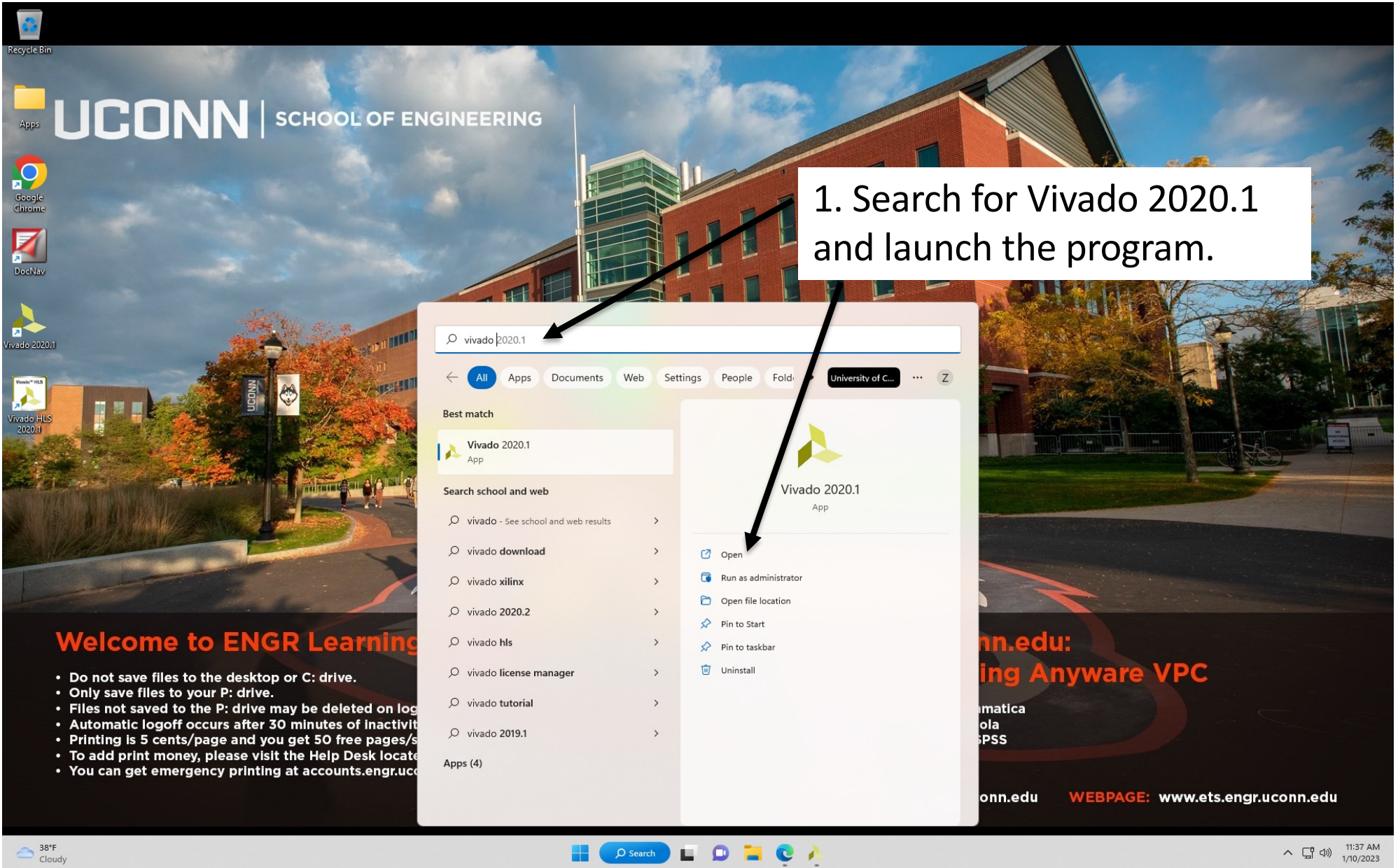
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Getting Started

At this point, it is assumed you either

1. Have Vivado downloaded on your personal computer
2. Are connected to an SoE computer via UConn Anyware
3. Are in E2 305/306/307 and are using one of the provided desktops

If you haven't already, go through the Vivado toolchain guide to get started with the software we will use.



2. Click 'Create Project' and hit 'Next.'

The screenshot shows the Vivado 2020.1 user interface. On the left, there is a sidebar with three main sections: 'Quick Start', 'Tasks', and 'Learning Center'. Under 'Quick Start', the 'Create Project >' option is highlighted with a black arrow. In the center, a 'New Project' dialog box is open. The dialog has a title bar 'New Project' and a close button. The main content area is titled 'Create a New Vivado Project' and contains the following text: 'This wizard will guide you through the creation of a new project. To create a Vivado project you will need to provide a name and a location for your project files. Next, you will specify the type of flow you'll be working with. Finally, you will specify your project sources and choose a default part.' At the bottom of the dialog, there are four buttons: '< Back', 'Next >', 'Finish', and 'Cancel'. A black arrow points to the 'Next >' button. The background of the interface is a light gray with blue and green accents.

Vivado 2020.1

File Flow Tools Window Help Q: Quick Access

VIVADO HLx Editions

XILINX

Quick Start

Create Project >
Open Project >
Open Example Project >

Tasks

Manage IP >
Open Hardware Manager >
XHub Stores >

Learning Center

Documentation and Tutorials >
Quick Take Videos >
Release Notes Guide >

3. Name project 'lab0' and select a save destination*, then click 'Next.'

Project Name

Enter a name for your project and specify a directory where the project data files will be stored.

Project name: lab0

Project location: C:/Users/zpd17002

Create project subdirectory

Project will be created at: C:/Users/zpd17002/lab0

< Back Next > Finish Cancel

*As of Jan 10, 2023, the P: drive is discontinued. When working on UConn Anyware / E2 computers, files saved at 'C:/Users/abc12345/...' **will remain saved** after logging off. If you plan on working on both personal and UConn computers, you should also consider saving to OneDrive. [Saving to OneDrive](#) will allow you to access files through a synced folder accessible through your personal computer and UConn Anyware desktop.

4. Choose RTL Project and click 'Next.'

Quick Start

- Create Project >
- Open Project >
- Open Example Project >

Tasks

- Manage IP >
- Open Hardware Manager >
- XHub Stores >

Learning Center

- Documentation and Tutorials >
- Quick Take Videos >
- Release Notes Guide >

New Project

Project Type
Specify the type of project to create.

- RTL Project**
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.
- Do not specify sources at this time
- Post-synthesis Project**
You will be able to add sources, view device resources, run design analysis, planning and implementation.
- Do not specify sources at this time
- JIO Planning Project**
Do not specify design sources. You will be able to view part/package resources.
- Imported Project**
Create a Vivado project from a Synplify, XST or ISE Project File.
- Example Project**
Create a new Vivado project from a predefined template.

? < Back Next > Finish Cancel

Tcl Console
New Project Wizard will guide you through the process of selecting design sources and a target device for a new project.

39°F Partly sunny

Search

11:54 AM 1/10/2023

Quick Start

- Create Project >
- Open Project >
- Open Example Project >

Tasks

- Manage IP >
- Open Hardware Manager >
- XHub Stores >

Learning Center

- Documentation and Tutorials >
- Quick Take Videos >
- Release Notes Guide >

New Project

Add Sources

Specify HDL, netlist, Block Design, and IP files, or directories containing those files, to add to your project. Create a new source file on disk and add it to your project. You can also add and create sources later.

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↑

↓

Create Source File

Create a new source file and add it to your project.

File type: VHDL

File name: lab0

File location: <Local to Project>

OK Cancel

Add Files Add Directories Create File

Scan and add RTL include files into project

Copy sources into project

Add sources from subdirectories

Target language: VHDL Simulator language: Mixed

? < Back Next > Finish Cancel

4. Click 'Create File' and configure it as shown.

5. Change target language to VHDL and click 'Next.'

Quick Start

- Create Project >
- Open Project >
- Open Example Project >

Tasks

- Manage IP >
- Open Hardware Manager >
- XHub Stores >

Learning Center

- Documentation and Tutorials >
- Quick Take Videos >
- Release Notes Guide >

New Project

Add Constraints (optional)
Specify or create constraint files for physical and timing constraints.

Use Add Files or Create File buttons below

Copy constraints files into project

6. Leave constraints blank for now and click 'Next.'



Quick Start

- Create Project >
- Open Project >
- Open Example Project >

Tasks

- Manage IP >
- Open Hardware Manager >
- XHub Stores >

Learning Center

- Documentation and Tutorials >
- Quick Take Videos >
- Release Notes Guide >

New Project

Default Part
Choose a default Xilinx part or board for your project.

Parts | Boards

Reset All Filters

Category: All Package: All Temperature: All
Family: All Speed: All Static power: All

Search: Q:

Part	I/O Pin Count	Available IOBs	LUT Elements	FlipFlops	Block RAMs	Ultra RAMs	DSPs	Gb Transceivers	GTPE2 Transceiv
xc7k70tffbg676-2L	676	300	41000	82000	135	0	240	8	0
xc7k70tffbg676-1	676	300	41000	82000	135	0	240	8	0
xc7k70tffbv484-3	484	285	41000	82000	135	0	240	4	0
xc7k70tffbv484-2	484	285	41000	82000	135	0	240	4	0
xc7k70tffbv484-2L	484	285	41000	82000	135	0	240	4	0
xc7k70tffbv484-1	484	285	41000	82000	135	0	240	4	0
xc7k70tffbv676-3	676	300	41000	82000	135	0	240	8	0
xc7k70tffbv676-2	676	300	41000	82000	135	0	240	8	0
xc7k70tffbv676-2L	676	300	41000	82000	135	0	240	8	0
xc7k70tffbv676-1	676	300	41000	82000	135	0	240	8	0
xc7k70tffbg484-2L	484	285	41000	82000	135	0	240	4	0

< Back Next > Finish Cancel

7. Keep default part and click 'Next.' Then, click 'Finish' on the next window.

Tcl Console
New Project Wizard will guide you through the process of selecting design sources and a target device for a new project.

lab0 - [C:/Users/zpd17002/lab0/lab0.xpr] - Vivado 2020.1

File Edit Flow Tools Reports Window Layout View Help Quick Access

Flow Navigator PROJECT MANAGER - lab0

PROJECT MANAGER

- Settings
 - Add Sources
 - Language Templates
 - IP Catalog
- IP INTEGRATOR
 - Open Block Design
 - Generate Block Design
- SIMULATION
 - Run Simulation
- PROGRAM AND DEBUG
 - Generate Bitstream
 - Open Hardware Manager

Sources

- Constraints
- Utility Sources

Project Summary

Overview | Dashboard

Settings Edit

Project name: lab0
Project location: C:/Users/zpd17002/lab0
Product family: Kintex-7
Project part: xc7k70ffbv676-1
Top module name: Not defined

Define Module

Define a module and specify I/O Ports to add to your source file.
For each port specified:
MSB and LSB values will be ignored unless its Bus column is checked.
Ports with blank names will not be written.

Module Definition

Entity name: lab0
Architecture name: Behavioral

I/O Port Definitions

Port Name	Direction	Bus	MSB	LSB
in	in	<input type="checkbox"/>	0	0

OK Cancel

Implementation

Status: Not started
Messages: No errors or warnings
Part: xc7k70ffbv676-1
Strategy: Vivado Implementation Defaults
Report Strategy: Vivado Implementation Default Reports
Incremental implementation: None

Timing

Run Implementation to see timing results

Power

Run Implementation to see power results

Tcl Console Messages Log Reports Design Runs

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy	Report Strategy
synth_1	constrs_1	Not started															Vivado Synthesis Defaults (Vivado Synthesis 2020)	Vivado Synthesis Default Reports (Vivado Synthesi
impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implementation 2020)	Vivado Implementation Default Reports (Vivado Im

39°F Partly sunny

Search

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8. Leave this part as is and click 'OK.' You will be adding the port definitions in the VHDL code later.



9. Double click 'lab0(Behavioral) (lab0.vhd)' to open the project file.

The screenshot displays the Vivado 2020.1 Project Manager interface. The 'Sources' pane on the left shows the project hierarchy with 'lab0(Behavioral) (lab0.vhd)' selected. A black arrow points to this file. The 'Source File Properties' pane for 'lab0.vhd' is open, showing it is enabled and located at 'C:/Users/zpd17002/lab0/lab0.srcs/sources_1/new/lab0.vhd'. The main editor window shows the VHDL code for the Behavioral architecture of 'lab0'. The code includes library declarations for IEEE and UNISIM, and the start of the 'entity lab0' and 'architecture Behavioral' blocks.

```
3  -- Engineer:
4  --
5  -- Create Date: 01/10/2023 12:11:01 PM
6  -- Design Name:
7  -- Module Name: lab0 - Behavioral
8  -- Project Name:
9  -- Target Devices:
10 -- Tool Versions:
11 -- Description:
12 --
13 -- Dependencies:
14 --
15 -- Revision:
16 -- Revision 0.01 - File Created
17 -- Additional Comments:
18 --
19 -----
20
21
22 library IEEE;
23 use IEEE.STD_LOGIC_1164.ALL;
24
25 -- Uncomment the following library declaration if using
26 -- arithmetic functions with Signed or Unsigned values
27 --use IEEE.NUMERIC_STD.ALL;
28
29 -- Uncomment the following library declaration if instantiating
30 -- any Xilinx leaf cells in this code.
31 --library UNISIM;
32 --use UNISIM.VComponents.all;
33
34 entity lab0 is
35 -- Port ( );
36 end lab0;
37
38 architecture Behavioral of lab0 is
39 ;
```

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy	Report Strategy
synth_1	constrs_1	Not started															Vivado Synthesis Defaults (Vivado Synthesis 2020)	Vivado Synthesis Default Reports (Vivado Synthesi
impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implementation 2020)	Vivado Implementation Default Reports (Vivado Im

lab0 - [C:/Users/zpd17002/lab0/lab0.xpr] - Vivado 2020.1

File Edit Flow Tools Reports Window Layout View Help Q- Quick Access

Flow Navigator PROJECT MANAGER - lab0

PROJECT MANAGER

- Settings
- Add Sources
- Language Templates
- IP Catalog
- IP INTEGRATOR
 - Create Block Design
 - Open Block Design
 - Generate Block Design
- SIMULATION
 - Run Simulation
- RTL ANALYSIS
 - Open Elaborated Design
- SYNTHESIS
 - Run Synthesis
 - Open Synthesized Design
- IMPLEMENTATION
 - Run Implementation
 - Open Implemented Design
- PROGRAM AND DEBUG
 - Generate Bitstream
 - Open Hardware Manager

Sources

- Design Sources (1)
 - BIT_ADDER(BHV) (lab0.vhd)
- Constraints
- Simulation Sources (1)
- Utility Sources

Source File Properties

lab0.vhd

Enabled

Location: C:/Users/zpd17002/lab0/lab0.srcs/sources_1/new

Type: VHDL

Library: xil_defaultlib

Size: 0.9 KB

Modified: Today at 12:16:41 PM

Copied to: C:/Users/zpd17002/lab0/lab0.srcs/sources_1/new

Read-only: No

General Properties

Tcl Console Messages Log Reports Design Runs

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy	Report Strategy
synth_1	constrs_1	Not started															Vivado Synthesis Defaults (Vivado Synthesis 2020)	Vivado Synthesis Default Reports (Vivado Synthesis 2020)
impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implementation 2020)	Vivado Implementation Default Reports (Vivado Implementation 2020)

```

1  -- Simulation Tutorial
2  -- 1-bit Adder
3
4  -- This is just to make a reference to some common things needed.
5  LIBRARY IEEE;
6  use IEEE.STD_LOGIC_1164.ALL;
7  use IEEE.NUMERIC_STD.ALL;
8
9  -- We declare the 1-bit adder with the inputs and outputs
10 -- shown inside the port().
11 -- This will add two bits together(x,y), with a carry in(cin) and
12 -- output the sum(sum) and a carry out(count).
13 end BIT_ADDER is
14   port (a, b, cin      : in  unsigned(0 downto 0);
15         sum, count     : out STD_LOGIC );
16 end BIT_ADDER;
17
18 -- This describes the functionality of the 1-BIT adder.
19 architecture BHV of BIT_ADDER is
20   signal temp : unsigned(1 downto 0); -- 'signal' refers to an internal bus
21 begin
22   -- Calculate the complete sum.
23   temp <= ('0' & a) + ('0' & b) + ('0' & cin); -- 's' concatenates 2 values.
24
25   -- Sum of the 1-BIT adder.
26   sum <= temp(0);
27
28   -- Carry out of the 1-BIT adder.
29   cout <= temp(1);
30 end BHV;
  
```

10. Copy + paste the code from 'lab0.vhd' starting at line 1. Design sources will now read 'BIT_ADDER(BHV) (lab0.vhd)'

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11. Click 'Add Sources' then 'Add or create simulation sources' to add the testbench.

The screenshot shows the Vivado 2020.1 interface. In the Project Manager, the 'Add Sources' button is highlighted. The 'Add Sources' dialog box is open, showing the 'Add or create simulation sources' option selected. The dialog also displays the Vivado logo and the Xilinx logo. The background shows the Project Summary and Design Runs panels.

Specify and/or create source files to add to the project

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy	Report Strategy
synth_1	constrs_1	Not started															Vivado Synthesis Defaults (Vivado Synthesis 2020)	Vivado Synthesis Default Reports (Vivado Synthesi
impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implementation 2020)	Vivado Implementation Default Reports (Vivado Im

lab0 - [C:/Users/zpd17002/ECE 3401/lab0/lab0.xpr] - Vivado 2020.1

File Edit Flow Tools Reports Window Layout View Help Q Quick Access Ready

Flow Navigator PROJECT MANAGER - lab0

PROJECT MANAGER

- Settings
 - Add Sources
 - Language Templates
 - IP Catalog
- IP INTEGRATOR
 - Create Block Design
 - Open Block Design
 - Generate Block Design
- SIMULATION
 - Run Simulation
- RTL ANALYSIS
 - Open Elaborated Design
- SYNTHESIS
 - Run Synthesis
 - Open Synthesized Design
- IMPLEMENTATION
 - Run Implementation
 - Open Implemented Design
- PROGRAM AND DEBUG
 - Generate Bitstream
 - Open Hardware Manager

Sources

- Design Sources (1)
 - BIT_ADDER(BHV) (lab0.vhd)
- Constraints
- Simulation Sources (1)
- Utility Sources

Project Summary

Overview | Dashboard

Settings Edit

Project name: lab0
Project location: C:/Users/zpd17002/ECE 3401/lab0

12. Click 'Create File,' name the file 'test0,' click 'OK,' then 'Finish.'

Add Sources

Add or Create Simulation Source

Specify simulation specific HDL files, or to your project.

Specify simulation set: sim_1

Create Source File

Create a new source file and add it to your project.

File type: VHDL

File name: test0

File location: <Local to Project>

OK Cancel

Add Files Add Directories Create File

Scan and add RTL include files into project
Copy sources into project
Add sources from subdirectories
Include all design sources for simulation

< Back Next > Finish Cancel

Not started
No errors or warnings
xc7k70tfov676-1
Vivado Implementation Defaults
Vivado Implementation Default Reports
None

Run Implementation to see timing results

Run Implementation to see power results

Tcl Console Messages Log Reports Design Runs x

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy	Report Strategy
synth_1	constrs_1	Not started															Vivado Synthesis Defaults (Vivado Synthesis 2020)	Vivado Synthesis Default Reports (Vivado Synthesis 2020)
impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implementation 2020)	Vivado Implementation Default Reports (Vivado Implementation 2020)

Specify and/or create source files to add to the project

33°F
Mix to stop

Search

10:12 AM
1/12/2023

lab0 - [C:/Users/zpd17002/ECE 3401/lab0/lab0.xpr] - Vivado 2020.1

File Edit Flow Tools Reports Window Layout View Help Q Quick Access

Ready

Flow Navigator PROJECT MANAGER - lab0

PROJECT MANAGER

- Settings
- Add Sources
- Language Templates
- IP Catalog
- IP INTEGRATOR
 - Create Block Design
 - Open Block Design
 - Generate Block Design
- SIMULATION
 - Run Simulation
- RTL ANALYSIS
 - Open Elaborated Design
- SYNTHESIS
 - Run Synthesis
 - Open Synthesized Design
- IMPLEMENTATION
 - Run Implementation
 - Open Implemented Design
- PROGRAM AND DEBUG
 - Generate Bitstream
 - Open Hardware Manager

Sources

Design Sources (1)

- BIT_ADDER(BHV) (lab0.vhd)
- Constraints
- Simulation Sources (1)
- Utility Sources

Project Summary

Overview | Dashboard

Settings Edit

Project name: lab0
 Project location: C:/Users/zpd17002/ECE 3401/lab0
 Product family: Kintex-7
 Project part: xc7k70tffv676-1
 Top module name: BIT_ADDER

Implementation

Status: Not started
 Messages: No errors or warnings
 Part: xc7k70tffv676-1
 Strategy: Vivado Implementation Defaults
 Report Strategy: Vivado Implementation Default Reports
 Incremental implementation: None

Timing

Run Implementation to see timing results

Power

Run Implementation to see power results

Define Module

Define a module and For each port specify MSB and LSB values. Ports with blank name are assumed to be 0.

The module definition has not been changed. Are you sure you want to use these values?

Yes No

Module Definition

Entity name: test0
 Architecture name: Behavioral

I/O Port Definitions

Port Name	Direction	Bus	MSB	LSB
in	in	<input type="checkbox"/>	0	0

OK Cancel

13. Click 'OK,' then 'Yes.'

Tcl Console Messages Log Reports Design Runs

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy	Report Strategy
synth_1	constrs_1	Not started															Vivado Synthesis Defaults (Vivado Synthesis 2020)	Vivado Synthesis Default Reports (Vivado Synthesis 2020)
impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implementation 2020)	Vivado Implementation Default Reports (Vivado Implementation 2020)

33°F Mix to stop

Search

10:15 AM 1/12/2023

lab0 - [C:/Users/zpd17002/ECE 3401/lab0/lab0.xpr] - Vivado 2020.1

File Edit Flow Tools Reprts Window Layout View Help Q- Quick Access

Flow Navigator PROJECT MANAGER - lab0

PROJECT MANAGER

- Settings
- Add Sources
- Language Templates
- IP Catalog

IP INTEGRATOR

- Create Block Design
- Open Block Design
- Generate Block Design

SIMULATION

- Run Simulation

RTL ANALYSIS

- Open Elaborated Design

SYNTHESIS

- Run Synthesis
- Open Synthesized Design

IMPLEMENTATION

- Run Implementation
- Open Implemented Design

PROGRAM AND DEBUG

- Generate Bitstream
- Open Hardware Manager

Sources

- Design Sources (1)
 - BIT_ADDER(BHV) (lab0.vhd)
- Constraints
- Simulation Sources (2)
 - sim_1 (2)
 - BIT_ADDER(BHV) (lab0.vhd)
 - test0(Behavioral) (test0.vhd)
- Utility Sources

Hierarchy Libraries Compile Order

Source File Properties

test0.vhd

- Enabled
- Location: C:/Users/zpd17002/ECE 3401/lab0/srcs/sim_1/new
- Type: VHDL
- Library: xil_defaultlib
- Size: 0.9 KB
- Modified: Today at 10:17:22 AM
- Copied to: C:/Users/zpd17002/ECE 3401/lab0/srcs/sim_1/new
- Read-only: No

General Properties

Project Summary test0.vhd

```
C:/Users/zpd17002/ECE 3401/lab0/srcs/sim_1/new/test0.vhd
3  -- Engineer:
4  --
5  -- Create Date: 01/12/2023 10:17:22 AM
6  -- Design Name:
7  -- Module Name: test0 - Behavioral
8  -- Project Name:
9  -- Target Devices:
10 -- Tool Versions:
11 -- Description:
12 --
13 -- Dependencies:
14 --
15 -- Revision:
16 -- Revision 0.01 - File Created
17 -- Additional Comments:
18 --
19
20
21
22 library IEEE;
23 use IEEE.STD_LOGIC_1164.ALL;
24
25 -- Uncomment the following library declaration if using
26 -- arithmetic functions with Signed or Unsigned values
27 --use IEEE.NUMERIC_STD.ALL;
28
29 -- Uncomment the following library declaration if instantiating
30 -- any Xilinx leaf cells in this code.
31 --library UNISIM;
32 --use UNISIM.VComponents.all;
33
34 entity test0 is
35 -- Port ( );
36 end test0;
37
38 architecture Behavioral of test0 is
39
```

14. Double click on 'test0(Behavioral) (test0.vhd)' to open the testbench.

Tcl Console Messages Log Reports Design Runs

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy	Report Strategy
synth_1	constrs_1	Not started															Vivado Synthesis Defaults (Vivado Synthesis 2020)	Vivado Synthesis Default Reports (Vivado Synthesi
impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implementation 2020)	Vivado Implementation Default Reports (Vivado Im

33°F Mix to stop

38:1 Insert VHDL

10:18 AM 1/12/2023

lab0 - [C:/Users/zpd17002/ECE 3401/lab0/lab0.xpr] - Vivado 2020.1

File Edit Flow Tools Reports Window Layout View Help Q Quick Access Ready

Flow Navigator PROJECT MANAGER - lab0

PROJECT MANAGER

- Settings
 - Add Sources
 - Language Templates
 - IP Catalog
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 - Create Block Design
 - Open Block Design
 - Generate Block Design
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 - Run Synthesis
 - Open Synthesized Design
- IMPLEMENTATION
 - Run Implementation
 - Open Implemented Design
- PROGRAM AND DEBUG
 - Generate Bitstream
 - Open Hardware Manager

Sources

Updating

Design Sources (1)

- BIT_ADDER(BHV) (lab0.vhd)

Simulation Sources (1)

- sim_1(1)
 - TEST_ADD(TEST) (test0.vhd) (1)

Utility Sources

Hierarchy Libraries Compile Order

Source File Properties

test0.vhd

Enabled

Location: C:/Users/zpd17002/ECE 3401/lab0/lab0.srcs/sim_1/new

Type: VHDL

Library: xil_defaultlib

Size: 4.4 KB

Modified: Today at 10:23:18 AM

Copied to: C:/Users/zpd17002/ECE 3401/lab0/lab0.srcs/sim_1/new

Read-only: No

General Properties

Project Summary test0.vhd

C:/Users/zpd17002/ECE 3401/lab0/lab0.srcs/sim_1/new/test0.vhd

```

1  -- 1-bit Adder Testbench
2
3  -- A testbench is used to functionally test a digital design.
4  -- The output of the testbench should allow the designer to see if
5  -- the design worked. The testbench should also report where the testbench
6  -- failed.
7
8  -- This is just to make a reference to some common things needed.
9  LIBRARY IEEE;
10 IEEE.STD_LOGIC_1164.ALL;
11 use IEEE.STD_LOGIC_1164.ALL;
12
13 -- Declare a testbench. Note that the testbench does not have any
14 -- input or output ports.
15 entity TEST_ADD is
16 end TEST_ADD;
17
18 -- Describes the functionality of the testbench.
19 architecture TEST of TEST_ADD is
20
21 -- The object that we wish to test is declared as a component of
22 -- the test bench. Its functionality has already been described elsewhere.
23 -- This simply describes what the object's inputs and outputs are, it
24 -- does not actually create the object.
25 component BIT_ADDER
26   port( a, b, cin      : in  unsigned;
27         sum, cout     : out STD_LOGIC );
28 end component;
29
30 -- Specifies which description of the adder you will use.
31 for U1: BIT_ADDER use entity WORK.BIT_ADDER (BHV);
32
33 -- Create a set of signals which will be associated with both the inputs
34 -- and outputs of the component that we wish to test.
35 signal A, B : unsigned(0 downto 0);
36 signal CIN : unsigned(0 downto 0);
37 signal SUM : STD_LOGIC;

```

15. Copy + paste the code from 'test0.vhd' starting at line 1. Simulation sources will now read 'TEST_ADD(TEST) (test0.vhd)(1)'

Tcl Console Messages Log Reports Design Runs

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy	Report Strategy
synth_1	constrs_1	Not started															Vivado Synthesis Defaults (Vivado Synthesis 2020)	Vivado Synthesis Default Reports (Vivado Synthesi
impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implementation 2020)	Vivado Implementation Default Reports (Vivado Im

136:10 Insert VHDL

33°F Mix to stop

Search

10:23 AM 1/12/2023

16. Click 'Run Simulation' then 'Run Behavioral Simulation.'

The screenshot shows the Vivado 2020.1 IDE. The 'Run' button in the left-hand 'SIMULATION' section is highlighted, and a context menu is open, showing 'Run Behavioral Simulation' as the selected option. A black arrow points from the text above to this menu item. The main workspace displays the 'test0.vhd' file, which contains VHDL code for a 1-bit adder testbench. The code includes library declarations, component declarations, and signal declarations. At the bottom, the 'Design Runs' table shows the status of various design runs.

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy	Report Strategy
synth_1	constrs_1	Not started															Vivado Synthesis Defaults (Vivado Synthesis 2020)	Vivado Synthesis Default Reports (Vivado Synthesi
impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implementation 2020)	Vivado Implementation Default Reports (Vivado Im

lab0 - [C:/Users/zpd17002/ECE 3401/lab0/lab0.xpr] - Vivado 2020.1

File Edit Flow Tools Repgrts Window Layout View Run Help Q- Quick Access

Flow Navigator

- PROJECT MANAGER
 - Settings
 - Add Sources
 - Language Templates
 - IP Catalog
- IP INTEGRATOR
 - Create Block Design
 - Open Block Design
 - Generate Block Design
- SIMULATION**
 - Run Simulation
- RTL ANALYSIS
 - Open Elaborated Design
- SYNTHESIS
 - Run Synthesis
 - Open Synthesized Design
- IMPLEMENTATION
 - Run Implementation
 - Open Implemented Design
- PROGRAM AND DEBUG
 - Generate Bitstream
 - Open Hardware Manager

SIMULATION - Behavioral Simulation - Functional - sim_1 - TEST_ADD

Scope x Sources

Name	Design U...	Block Type
TEST_ TEST_ADD		VHDL Entity
U1 BIT_ADDER		VHDL Entity

Objects x Protocol Inst

Name	Value	Data Type
A[0:0]	1	Array
B[0:0]	0	Array
CIN[0:0]	0	Array
SUM	1	Logic
COUT	0	Logic

test0.vhd x Untitled 1 x

Zoom Fit

Name	Value
A[0:0]	1
B[0:0]	0
CIN[0:0]	0
SUM	1
COUT	0

0.000 ns 200.000 ns 400.000 ns 600.000 ns 800.000 ns

16. The waveform window will automatically open. Click the 'Zoom Fit' icon to expand the time axis. Verify the output waveform.

Tcl Console x Messages Log

```

INFO: [USF-XS1m-96] XSim completed. Design snapshot 'TEST_ADD_behav' loaded.
INFO: [USF-XS1m-97] XSim simulation ran for 1000ns
launch_simulation: Time (s): cpu = 00:00:05 ; elapsed = 00:00:06 . Memory (MB): peak = 1024.195 ; gain = 0.000
  
```

Type a Tcl command here

Zoom Fit

33°F Mix to stop

Search

Questions

1. In BIT_ADDER(BHV) (lab0.vhd) what ...
 - a. is the purpose of the 'entity' declaration (line 13)?
 - b. is the purpose the 'architecture' declaration (line 19)?

2. In TEST_ADD(TEST) (test0.vhd)(1)...
 - a. what is the purpose of the 'component' declaration (line 25)?
 - b. what line # imports the functionality of the bit adder?
 - c. once the bit adder becomes instantiated, what line # maps the declared signals to the input/output ports of the adder?

Deliverables

Please submit a single PDF of the following:

1. A screenshot of the window shown in the slide 19
2. Your answers to the questions in slide 20