1. Implement the following logic functions as single CMOS logic gates. Draw out the entire schematic showing the nMOS and pMOS transistors for each function.

\[ Z = \overline{AB} (C + \overline{AB}) \]

\[ Z = D + A(B + C) \]

\[ Z = \overline{A}(D + E) \cdot BC \]

2. Select gate sizes x and y for minimum delay from A to B.

3. (a) What function do the following two circuits implement? (b) Circuit B does not have a dual as a the pull-up circuitry. Will this logic gate actually work? Why or why not? (c) Is there any advantage to the B topology versus A?