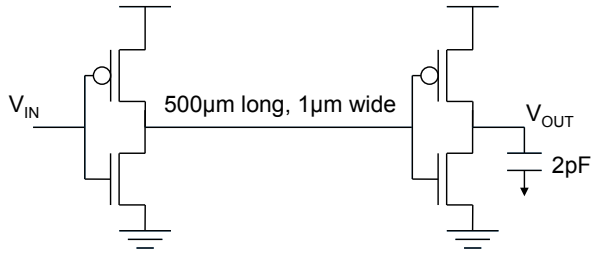
ECE 3421 – VLSI Design and Simulation, Spring 2013

Homework Assignment 3

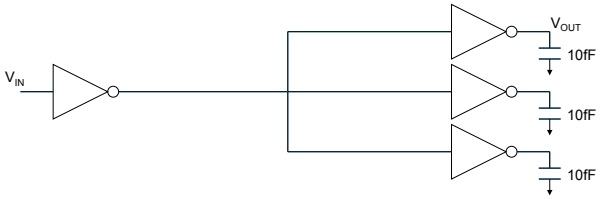
1. (a). What is the delay from V_{IN} to V_{OUT} in the following circuit. Assume that the wire resistance is 0.06 Ω/□ and the wire capacitance is 0.07 fF/μm^2. The equivalent resistance for the NMOS and PMOS transistors are 13 kΩ and 31 kΩ respectively. Assume that the input capacitance is 5 fF for a minimum sized transistor.



(b). If you scale the second inverter by a factor of 2, what happens to the delay time? Note that scaling the second inverter will decrease its equivalent resistance and increase its intrinsic capacitance.

(c) If you keep on scaling the second inverter, what trends do you expect to observe for the delay? Explain qualitatively.

2. Given the following circuit, estimate the delay time from V_{IN} to V_{OUT}. For all inverters, the equivalent resistance is 10 kΩ, and the input capacitance of each inverter is 10 fF. (hint: use Elmore delay model)



3. Given the following circuit, estimate the delay time from V_{IN} to V_{OUT}. For all inverters, the equivalent resistance is 10 kΩ, and the input capacitance of each inverter is 10 fF. The wire resistance is 0.06 Ω/□ and the wire capacitance is 0.07 fF/μm^2.