

ECE 3421 – VLSI Design and Simulation, Spring 2013

LVS

1. Introduction

Once you have created the layout as well as the schematic for a design, how do we know they represent the same circuit? One way to verify this is by generating a circuit netlist from the layout and comparing it with the netlist for the schematic. This is the essence of the LVS tool.

2. Layout Extraction

In order to use the LVS tool, we have to first extract the layout to the netlist.

[STEP 1:] In the Layout window, click on NCSU → Modify LVS Rules. Select "Compare FET Parameters" and click OK. Then, click on Verify → Extract. The Extractor window would pop up as in Figure 1 shows. Leave Switch Names empty and click on OK.

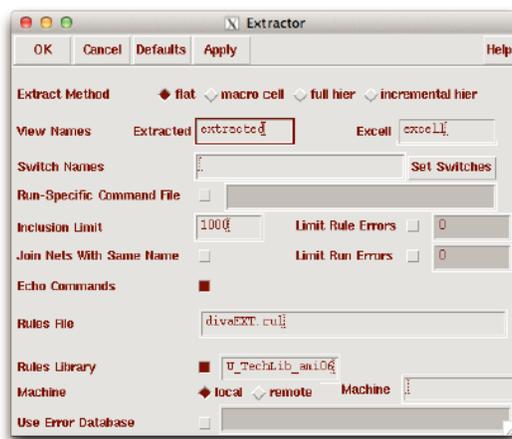


Figure 1: Layout Extractor Window.

[STEP 2:] Check the CIW window to make sure the layout extraction process runs through successfully as in Figure 2.

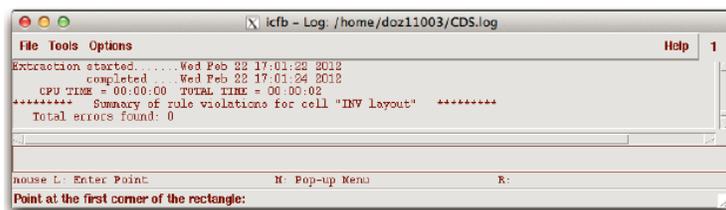


Figure 2: Check the Layout Extractor Result.

After the process finished check the cell in the Library manager and you will see an extracted view. Open it and a new Layout window appears showing the extracted layout as in Figure 3.

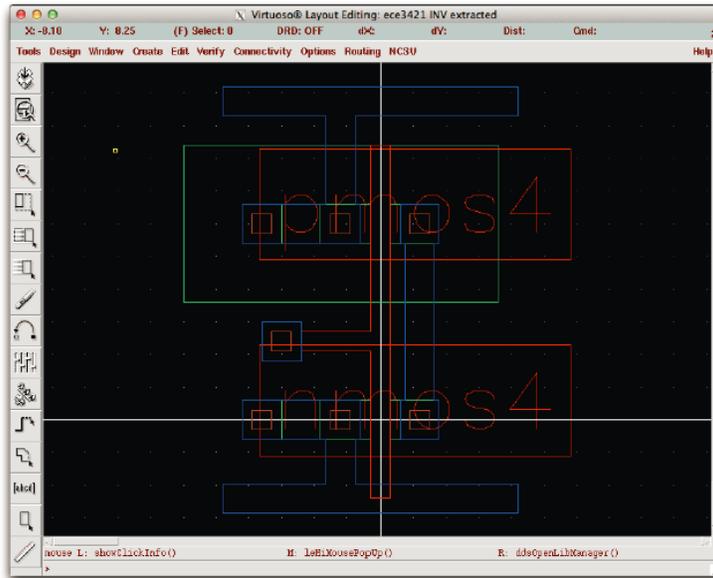


Figure 3: The Extracted Layout.

3. Layout Versus Schematic

[STEP 1:] From the layout window, choose Verify → LVS. The dialog box would appear as in Figure 4.

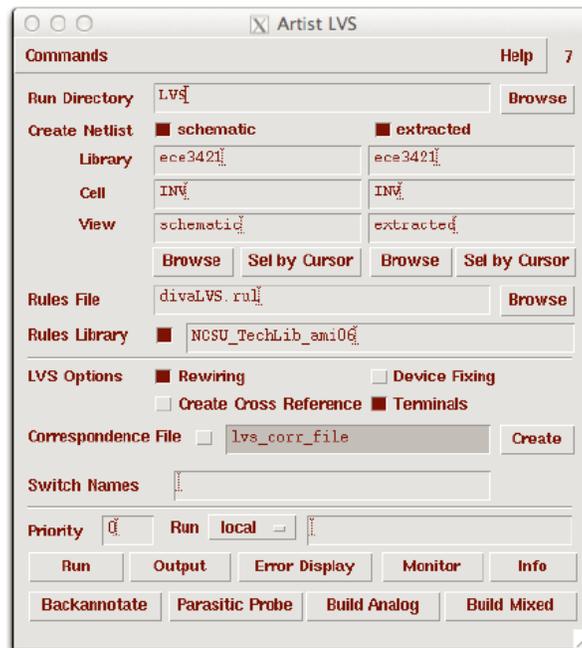


Figure 4: Artist LVS Window.

Specify the Run Directory as well as the Cell and View you want to compare using the corresponding Browse button. If you are running LVS on a very large layout, it is better to create a run directory on a spare disk so that LVS won't run out of disk space.

Make sure that you have choose the correct Rules File and Library by check the box beside it. If you already have executed an LVS under the specified directory before, a window will pop-up which might say "The selected LVS rule directory does not match the run form". Just click on Form contents and OK.

[STEP 2:] Click on the Run button. The LVS process may take a while to complete. To see if the job is still running, you can click on the Job Monitor button in the LVS window and a pop up menu will appear to tell you the status of the current process. If the process is not successful, you can click on Info in the LVS window. A "Display Run Information" window appears. You can check the log file to figure out the run time problem for LVS.

[STEP 3:] When the LVS finishes running, a window will popup indicating that the LVS has completed, shown in Figure 5.

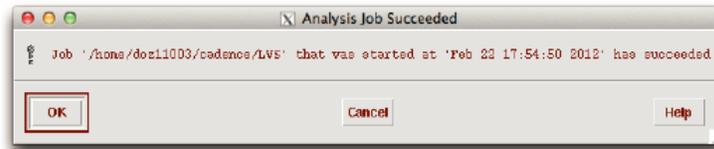


Figure 5: The N-diffusion (Active) Box.

If the LVS runs through successfully, click on Output in the LVS window and the result is displayed as below.

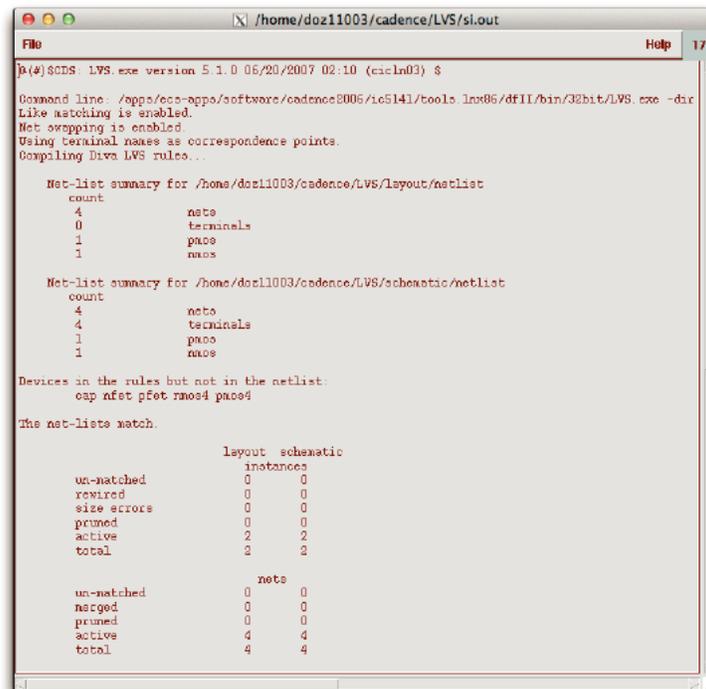


Figure 6: LVS Matching Result.

Note:

In some cases, even the netlist is matched, there may be still some mismatched parameters because of some differences in transistor sizing in the schematic and layout. Then you can click on the Error Display button in the LVS window to identify where in the layout the errors are.

In the Error Display window, click on First or other buttons to display the current or all the errors in the extracted layout window. The errors are highlighted by a green dot. To get more information about the error, click on the Explain button.

Modify the layout or schematic appropriately and rerun the LVS till your design is perfectly matched.