The figure 1 shows the logic diagram for a NOR gate.

1. Design a schematic for this circuit in cadence using \( W_n = W_p = 2\mu m \), and \( L = 0.6\mu m \) for both NMOS and PMOS transistors.
2. Make a symbol for this circuit.
3. To test your circuit, plot the input output characteristics.

![NOR Gate Diagram](image)

**C = \text{A NOR B}**

Figure 1: A two input NOR gate.

**Assignment**

1. Create a schematic for the above NOR gate in cadence.
2. Turn in the Input/output waveform showing all possible input combinations of A & B.
3. What is the worst-case propagation delay and for which input combination? Why do propagation delays vary for different input combinations?
4. Ideally, how fast can this gate can be driven with a load of 1pF capacitor? Show the output waveform of this case. (Hint: The output needs to reach a stable value after each transition.)